

CR-1 : @FROSTBURG_FABC.LB\FROSTBURG_FABC\SCH_1\PAGE1		6	5	4	3	2	1							
D	PAGE #	COMPONENT/FUNCTION	PAGE #	COMPONENT/FUNCTION	PAGE #	COMPONENT/FUNCTION	REVISIONS							
	[1.	INDEX]	[50.	PCI TERMINATION]			REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
	[2.	BLOCK DIAGRAM]	[51.	STD FRONT PANEL HDR]			2.02	DESIGN		2006				
	[3.	RESET MAP]	[52.	USB_FP_HEADER_POWER]										
	[4.	CLOCK DISTRIBUTION]	[53.	1394 CONTROLLER]										
	[5.	GPIO, IRQ, IDSEL MAP]	[54.	1394 BP REV1]										
	[6.	CPU-SOCKET 1 OF 2]	[55.	1394 PWR/DCPL]										
	[7.	CPU SOCKET 2 OF 2]	[56.	LAN NINEVEH]										
	[8.	CPU TERMINATION & MISC P/U P/D]	[57.	LAN NINEVEH]										
	[9.	CPU PLL FILTERED SUPPLY]	[58.	LAN NINEVEH]										
	[10.	MCH SECTIONS PAGE 1 OF 6]	[59.	AUDIO CODEC]										
	[11.	MCH SECTIONS PAGE 2 OF 6]	[60.	AUDIO DECOUPLING & JACK SENSE]										
	[12.	MCH SECTIONS PAGE 3 OF 6]	[61.	AUDIO SPDIF]										
	[13.	MCH SECTIONS PAGE 4 OF 6]	[62.	AUDIO JACK (BLUE GREEN PINK]										
C	[14.	MCH SECTIONS PAGE 5 OF 6]	[63.	AUDIO JACK (BLACK ORANGE]										
	[15.	MCH SECTIONS PAGE 6 OF 6]	[64.	AUDIO FP HEADERS & HDA HEADER]										
	[16.	PLL & CRT FILTERS]	[65.	AUDIO MIC BIAS]										
	[17.	MCH DECOUPLING AND COMP]	[66.	AUDIO VREG]										
	[18.	MCH DCPL & VGA TERMINATION]	[67.	SPDIF HEADER]										
	[19.	MCH VREFS & TERMINATION]	[68.	TPM 1.2]										
	[20.	VGA CONNECTOR]	[69.	PORT ANGELES 1 OF 2]										
	[21.	PCI EXPRESS X16]	[70.	PORT ANGELES 2 OF 2]										
	[22.	PCI EXPRESS X16]	[71.	FDD CONN]										
	[23.	PCI EXPRESS X16 COUPLING]	[72.	PS/2 CONNECTOR]										
	[24.	240P CONN DDR2, CH A]	[72.	LPT SIGNALS]										
	[25.	240P CONN DDR2, CH B]	[73.	LPT SIGNALS]										
	[26.	DDR VTT TERMINATION]	[74.	SERIAL PORT A]										
B	[27.	DDR VTT DECOUPLING]	[75.	STUDIES PURPOSE]										
	[28.	CK505 PAGE 1 OF 2]	[76.	SST SENSOR]										
	[29.	CK505 PAGE 2 OF 2]	[77.	FAN CONFIGURATION]										
	[30.	ICH9 1 OF 6 CONTROL]	[78.	MTG HOLES/LABELS]										
	[31.	ICH9 2 OF 6 CONTROL]	[79.	CORE VREG]										
	[32.	ICH9 3 OF 6 CONTROL]	[80.	CORE VREG]										
	[33.	ICH9 4 OF 6 - CONTROL]	[81.	VREG_SM_VTT]										
	[34.	ICH 5 OF 6 - CONTROL]	[82.	VREG_1P25_CORE MCH]										
	[35.	ICH 6 OF 6 - GROUND BODY]	[83.	MCH DCPL]										
	[36.	GPIO TERMINATION & RST STRAPS]	[84.	CORE VREG]										
	[37.	ICH PIN STRAPS]	[85.	VREG_FSB VTT & SFR]										
	[38.	ICH DECOUPLING]	[86.	VREG 1.25 MCH CL]										
	[39.	ME & CONTROL BUFFERS/ICH CIRCUITS]	[87.	CORE VREG]										
	[40.	SERIAL FLASH PRIMARY]	[88.	CORE VREG]										
A	[41.	SATA CONNECTORS]	[89.	CORE VREG]										
	[42.	USB FP HDR 1]	[90.	NO PAGE TITLE FOUND!!!]										
	[43.	USB FP HDR 2]	[91.	WAKE CONTROL SWITCH PS2/USB (BP RIGHT)]										
	[44.	USB FP HDR 2]	[92.	VREG: DECOUPLING AND STITCHING]										
	[45.	BACK PANEL USB]	[93.	VCCP VREG]										
	[46.	BACK PANEL USB WITH ESATA]	[94.	VCCP VREG]										
	[47.	PCI EXPRESS X1 #1]	[95.	VCCP VREG]										
	[48.	PCI CONN 1]	[96.	VREG: VCCP DECOUPLING / 2X2 CONN]										
	[49.	PCI CONN 2]												
8		7	6	5	4	3	2	1						

BEARLAKE-B ATX

CLASSIC SKU

FROSTBURG

DRAGONTAIL PEAK

FAB C

TAPE-OUT: WWXX-2006

FAB A REV 3.03

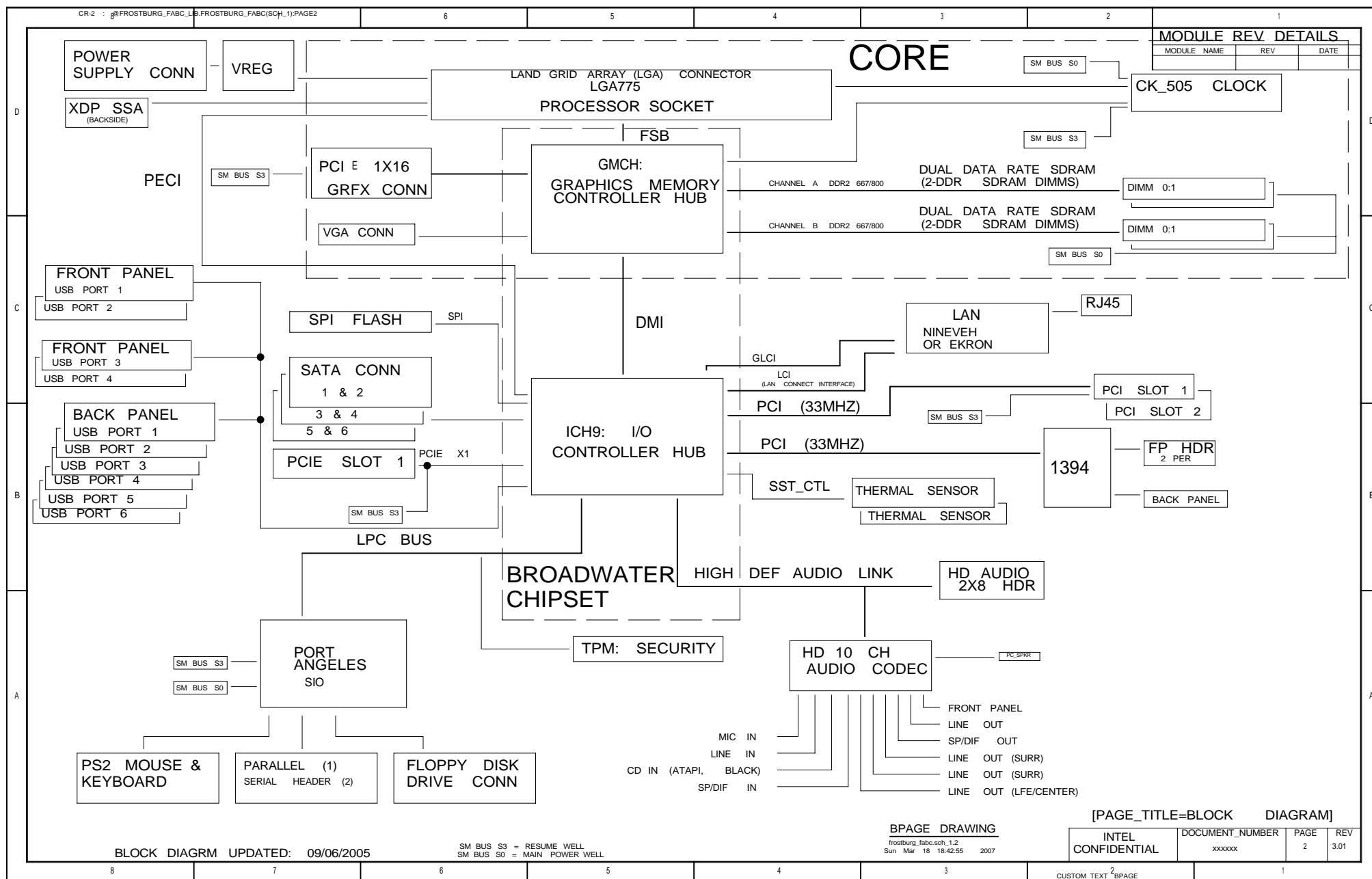
CONROE, BEARLAKE, DDR?, ICH9,
2-CHANNEL DDR2, PCIEXPRESS GFX, ATX
CUSTOMER REFERENCE BOARD

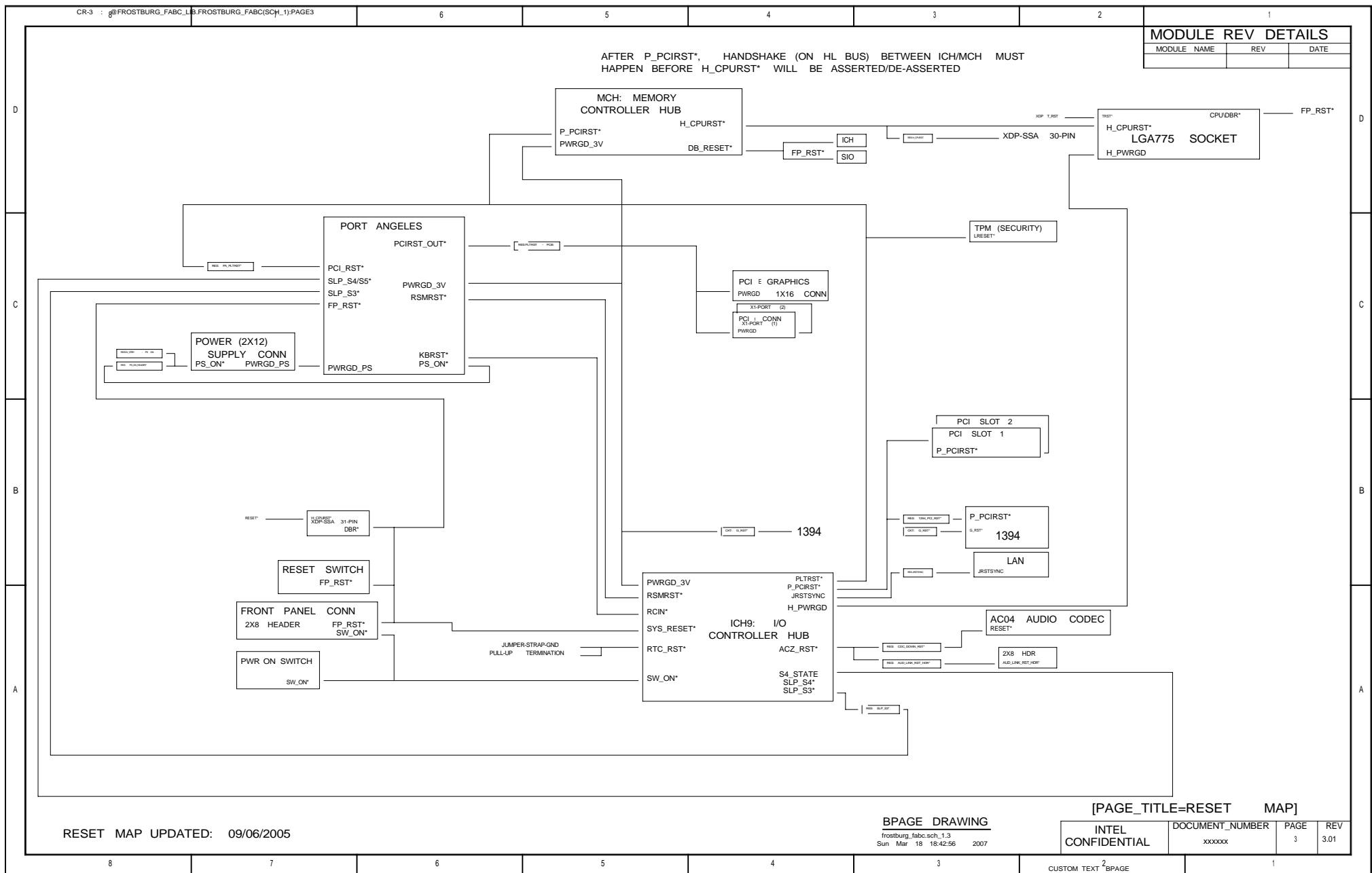
POWER SYMBOLS USED:
VCC3
VCC
+12V
-12V

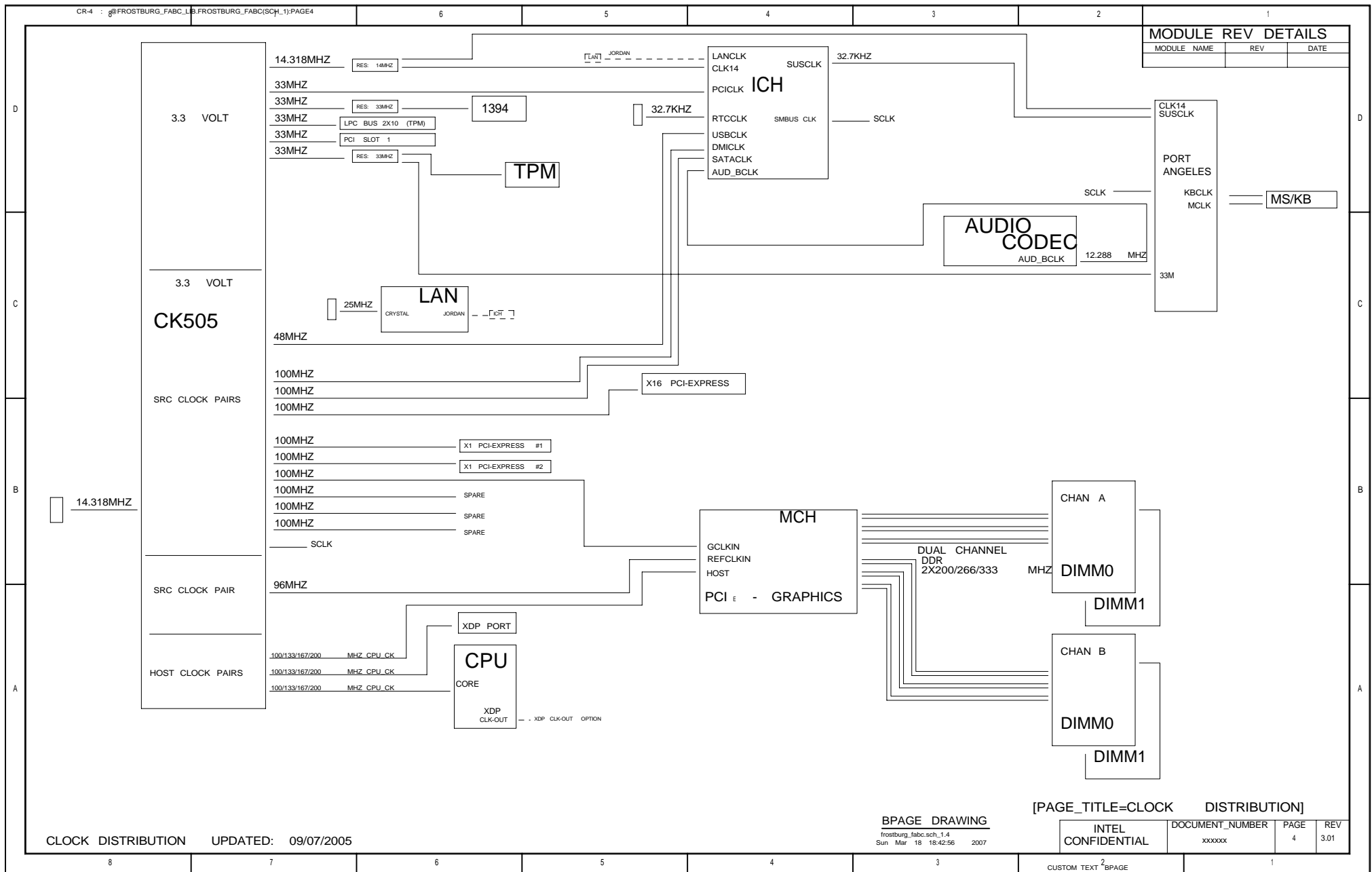
NOTES:
1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPL'S FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

BOM_RELEASE_DATE	1	PB_NUMBER	1
SIGNATURE	DATE	inte3065 BOWERS AVE SANTA CLARA, CA 95051	
DRN_BY	1	TITLE	
CHK_BY	1	?	
ENGR_APVD	1		
CUSTOM TEXT B-PAGE		INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx
		PAGE 1/107	REV 3.01

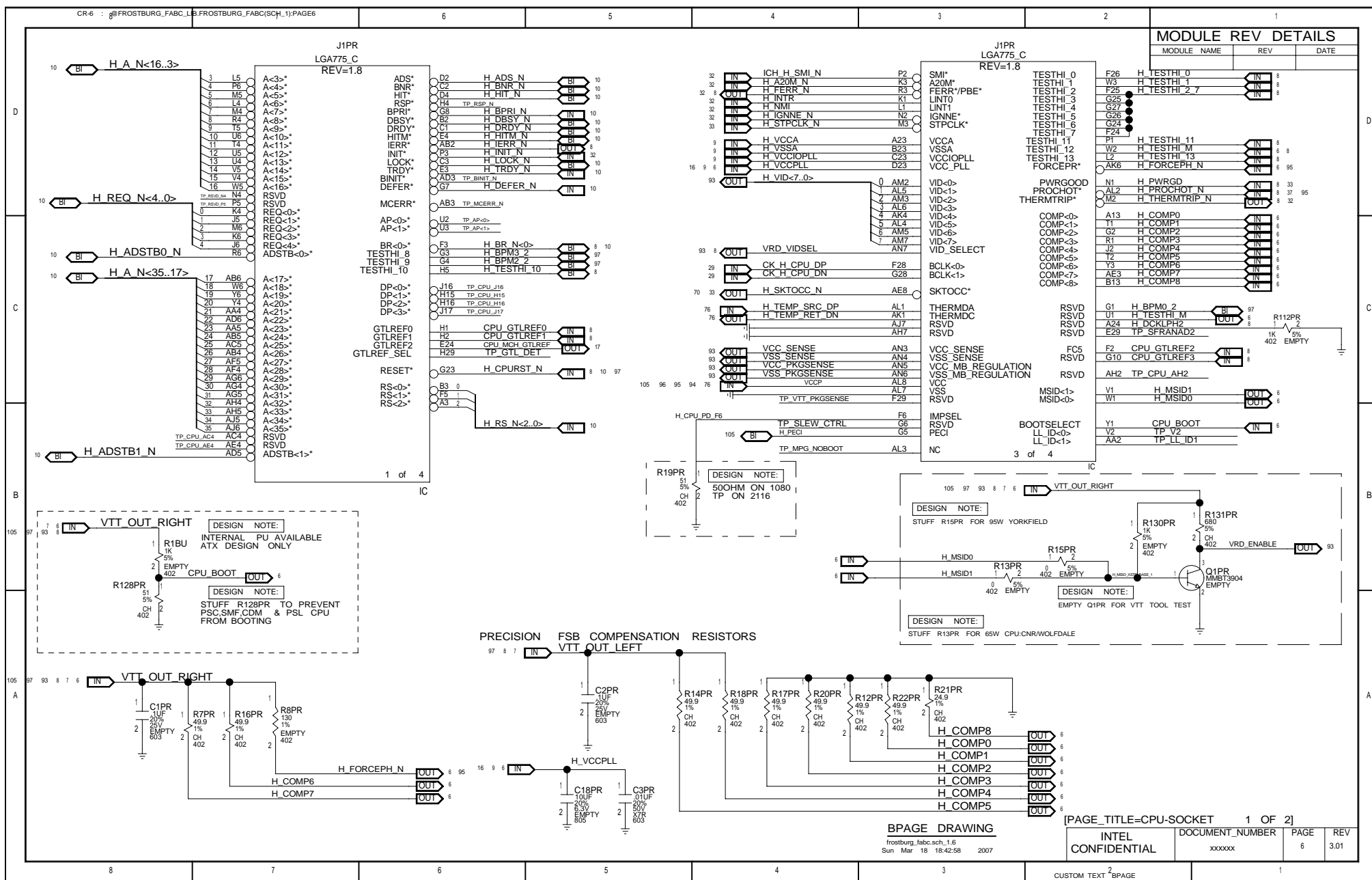
[PAGE_TITLE=INDEX]
BPAGE DRAWING
frostburg_fabc.sch_1.1
Sun Mar 18 18:42:55 2007

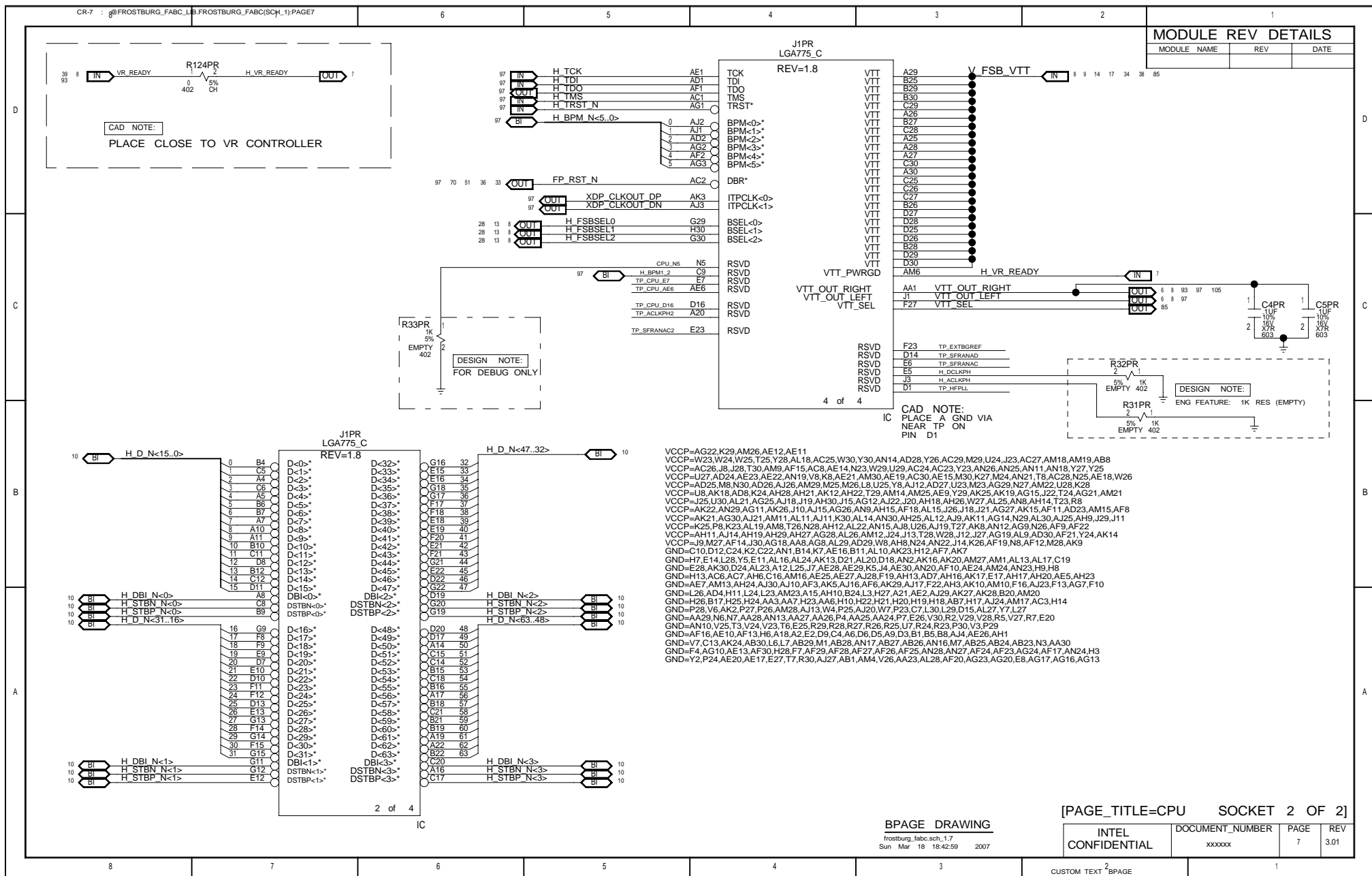


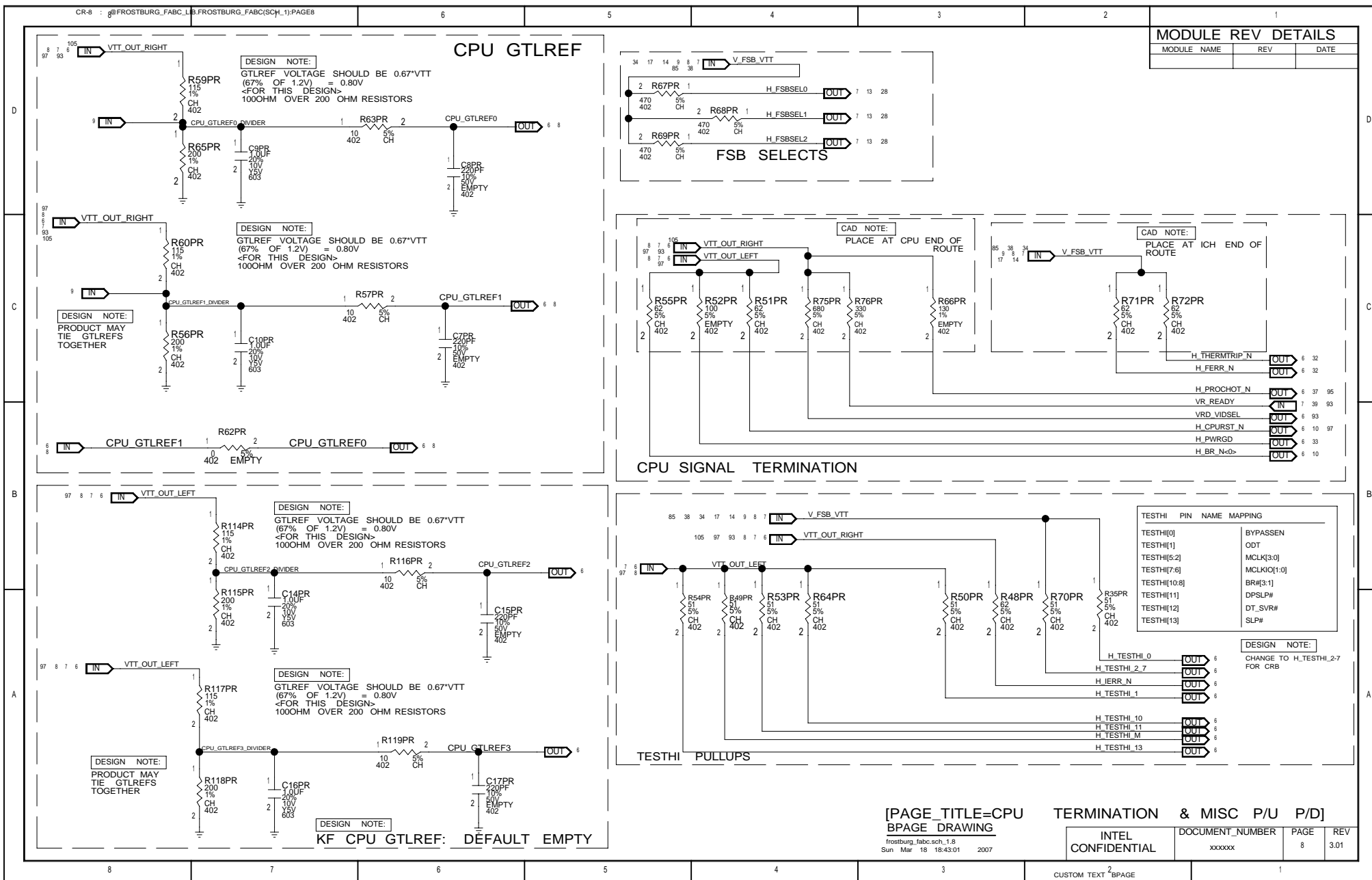


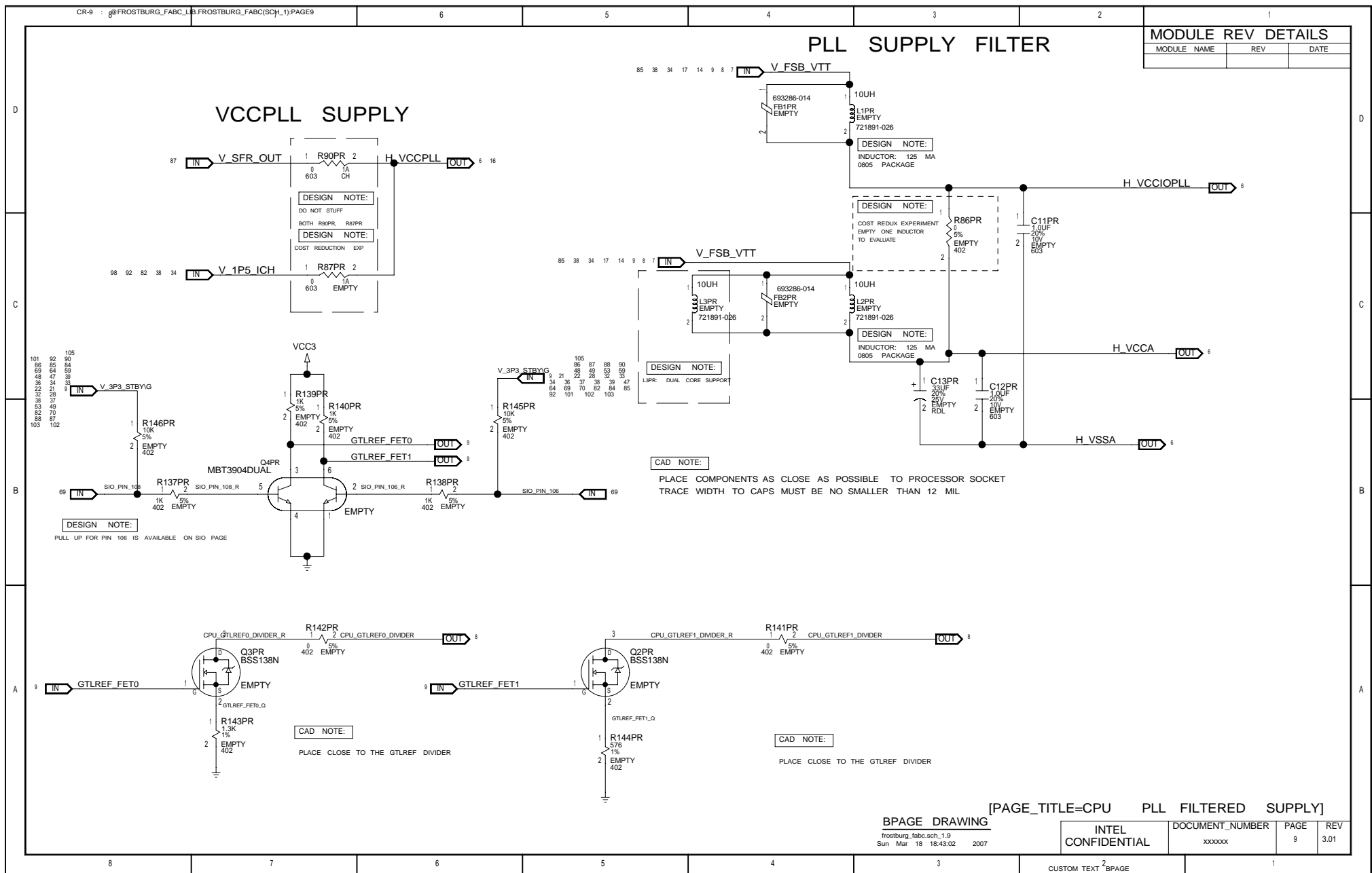


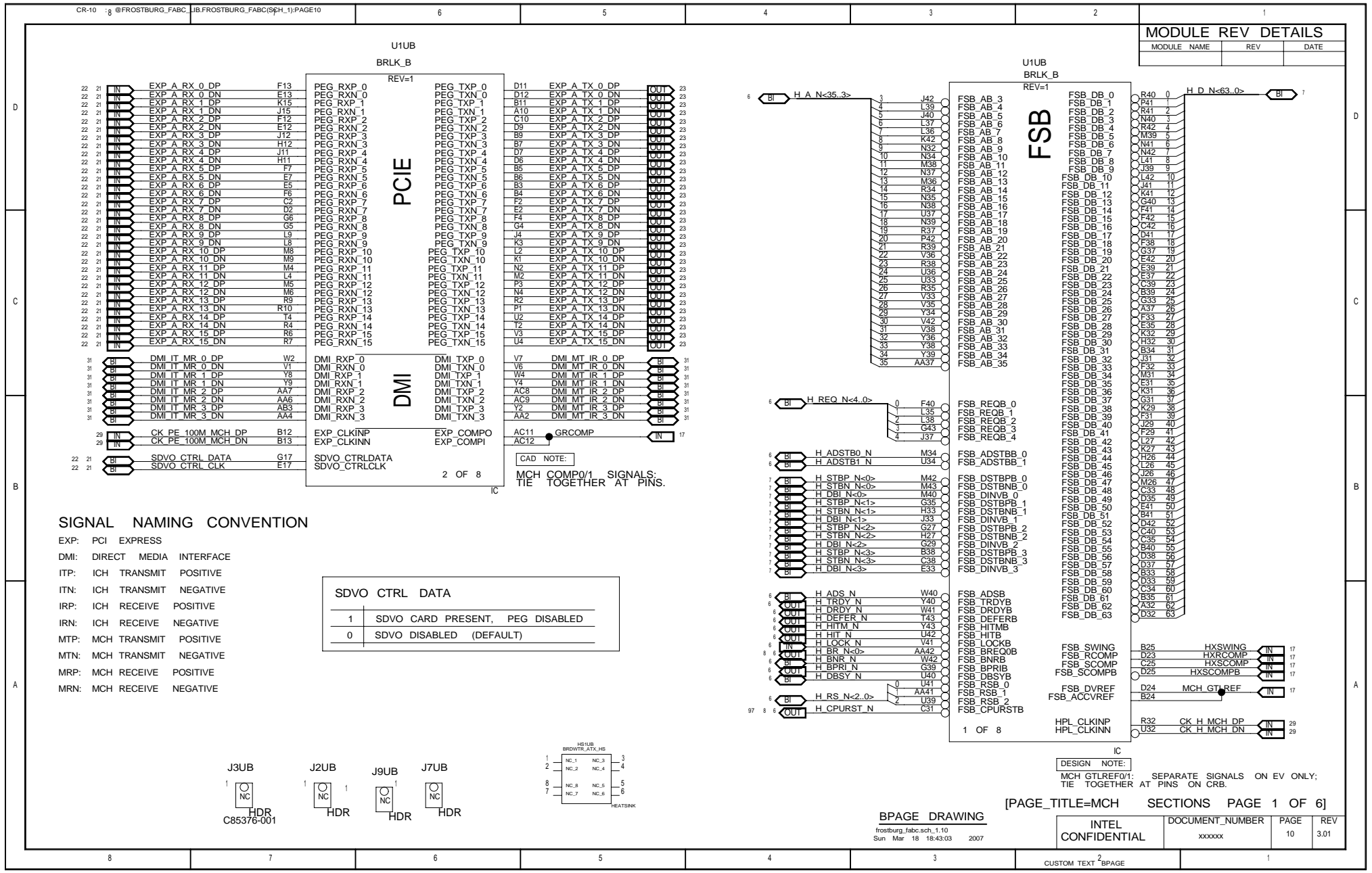
CR-5 : g@FROSTBURG_FABC_LB\FROSTBURG_FABC(SCH_1):PAGE5										6	5	4	3	2	1	
ICH										GPIO SIGNALS NOT USED: GP40-47	MODULE REV DETAILS					
										S3/S5	NOTES	MODULE NAME	REV	DATE		
PIN NAME										POWER WELL	USAGE	AFTER PLTRST				
GP[0]										MAIN (CORE)	FP AUD DETECT	IN				
GP[1]										MAIN (CORE)	FRONT FAN TACH	IN				
GP[2]										MAIN (CORE)	P_INTF	IN				
GP[3]										MAIN (CORE)	P_INTF	IN				
GP[4]										MAIN (CORE)	P_INTG	IN				
GP[5]										MAIN (CORE)	P_INTH	IN				
GP[6]										MAIN (CORE)	REAR FAN TACH	IN				
GP[7]										MAIN (CORE)	EV FAN TACH	IN				
GP[8]										RESUME (STBY)	SATA/HOT-SWAP	IN				
GP[9]										RESUME (STBY)	WOL	OUT				
GP[10]										RESUME (STBY)	NOT USED (RVP)	OUT				
GP[11]										RESUME (STBY)	PORT 80 LED	OUT(ALERT)				
GP[12]										RESUME (STBY)	BOARD ID 3	IN				
GP[13]										RESUME (STBY)	LPC_SIO_PME	IN				
GP[14]										RESUME (STBY)	NOT USED (RVP)	IN				
GP[15]										RESUME (STBY)	LAN DISABLE	OUT				
GP[16]										MAIN (CORE)	BOARD ID 1	IN				
GP[17]										MAIN (CORE)	CPU FAN TACH	IN				
GP[18]										MAIN (CORE)	BOARD ID 2	IN				
GP[19]										MAIN (CORE)	SATA1GP	IN				
GP[20]										MAIN (CORE)	NOT USED (TP: SATA HOTSWAP CTL)	OUT				
GP[21]										MAIN (CORE)	SATA0GP	IN				
GP[22]										MAIN (CORE)	NOT USED	IN				
GP[23]										MAIN (CORE)	LDRQ1	OUT				
GP[24]										RESUME (STBY)	V_SM LED CONTROL	OUT				
GP[25]										RESUME (STBY)	BOARD ID 4	IN				
GP[26]										RESUME (STBY)	S4_STATE	OUT				
GP[27]										RESUME (STBY)	NOT USED (TP)	LOW				
GP[28]										RESUME (STBY)	NOT USED (TP)	LOW				
GP[29]										RESUME (STBY)	OC5	IN				
GP[30]										RESUME (STBY)	OC6	IN				
GP[31]										RESUME (STBY)	OC7	IN				
GP[32]										MAIN (CORE)	BOARD ID 0	IN				
GP[33]										MAIN (CORE)	MFG_MODE (RVP)	IN				
GP[34]										MAIN (CORE)	ICH_CFG_JUMPER	IN				
GP[35]										MAIN (CORE)	NOT USED (TP)	IN				
GP[36]										MAIN (CORE)	SATA2GP	IN				
GP[37]										MAIN (CORE)	SATA3GP	IN				
GP[38]										MAIN (CORE)	NOT USED	IN				
GP[39]										MAIN (CORE)	NOT USED	IN				
GP[48]										MAIN (CORE)	NOT USED	IN				
GP[49]										CPU	CPUPWRGD	IN				
PORT ANGELES										(BASED ON NATIONAL PA3.0, MAY 2004, REV 1.1; MULTI-PLEXED/PROGRAMMABLE GPIO PINS)						
GPXX (PIN 103/118)										STBY/VCC3	NOT USED (TP)	I/O				
GPXX (PIN 104/119)										STBY/VCC3	1394_ENABLE	I/O				
GPXX (PIN 105/120)										STBY/VCC3	NOT USED (TP)	I/O				
GPXX (PIN 106/121)										STBY/VCC3	1_WATT_VREG_CONTROL	I/O				
GPXX (PIN 108/124)										STBY/VCC3	1_WATT_VREG_CONTROL+	I/O				
GPXX (PIN 109/126)										STBY/VCC3	MEM. OVERVOLTAGE_CONTROL1	I/O				
GPXX (PIN 111/127)										STBY/VCC3	MEM. OVERVOLTAGE_CONTROL (TP)	I/O				
GPXX (PIN 112/128)										STBY/VCC3	BOARD ID 5	I/O				
GPXX (PIN 116)										STBY	5V_DDCSDA	I/O				
GPXX (PIN 114)										STBY	5V_DDCSCL	I/O				
GPXX (PIN 74/115/122)										STBY/STBY/VCC3	3V_DDCSDA	I/O				
GPXX (PIN 75/113/125)										STBY/STBY/VCC3	3V_DDCSCL	I/O				
GPXX (PIN 101)										STBY	2X12_HDR_DETECT	I/O				
GPXX (PIN 100)										STBY	NOT USED (TP)	I/O				
GPXX (PIN 102)										N/C (PA30)	NOT USED (PA30)	N/C (PA30)				

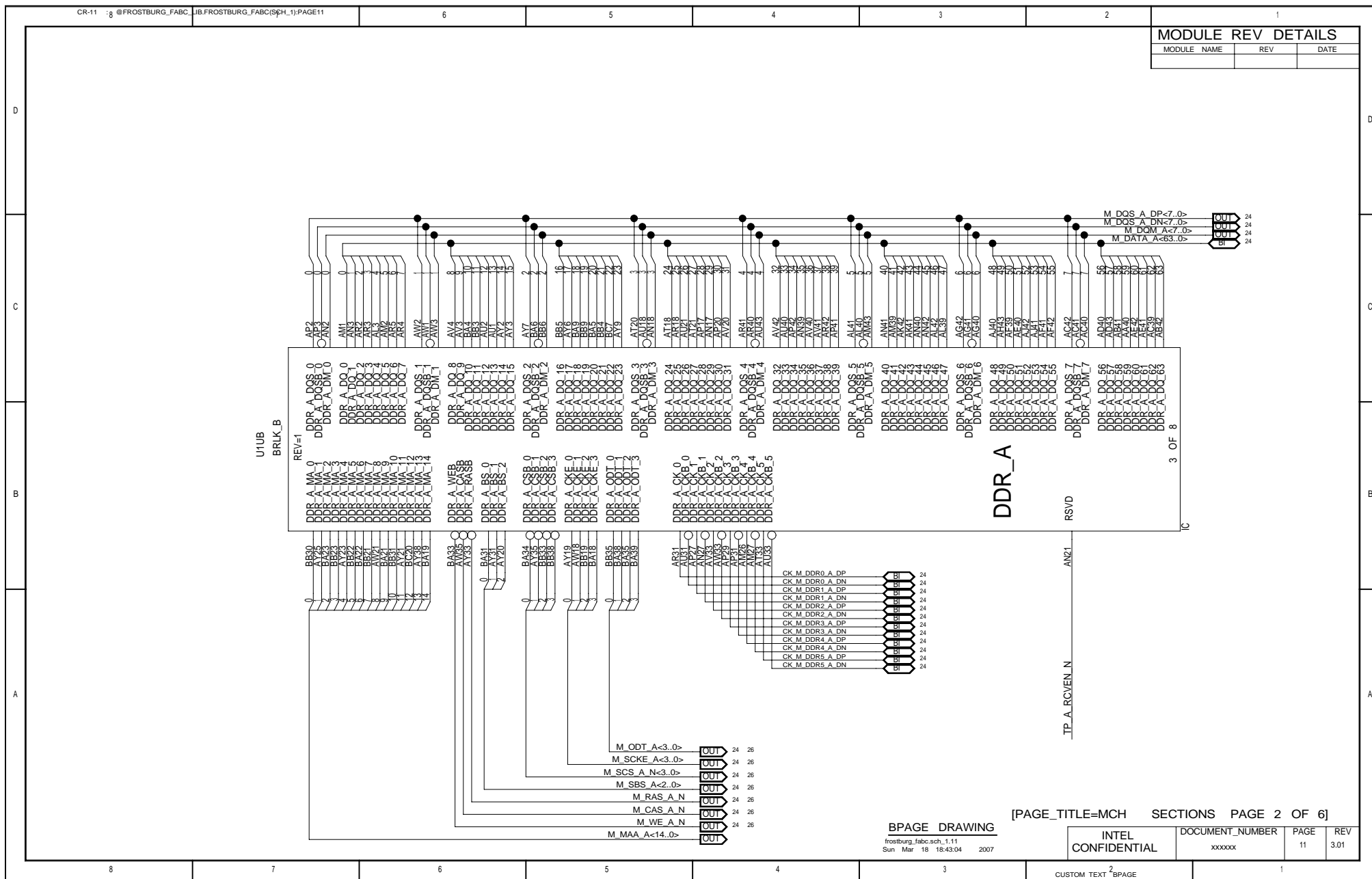


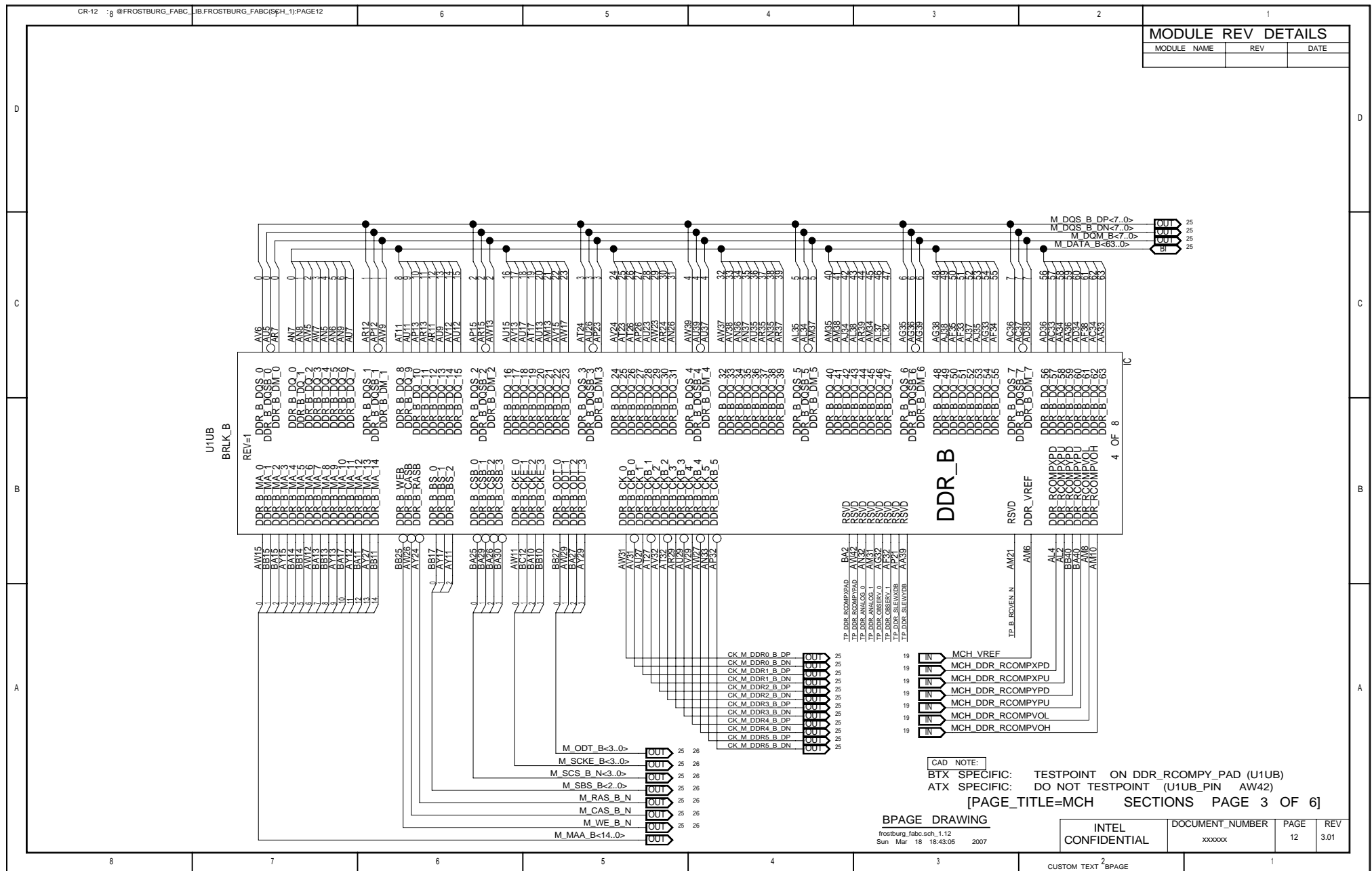


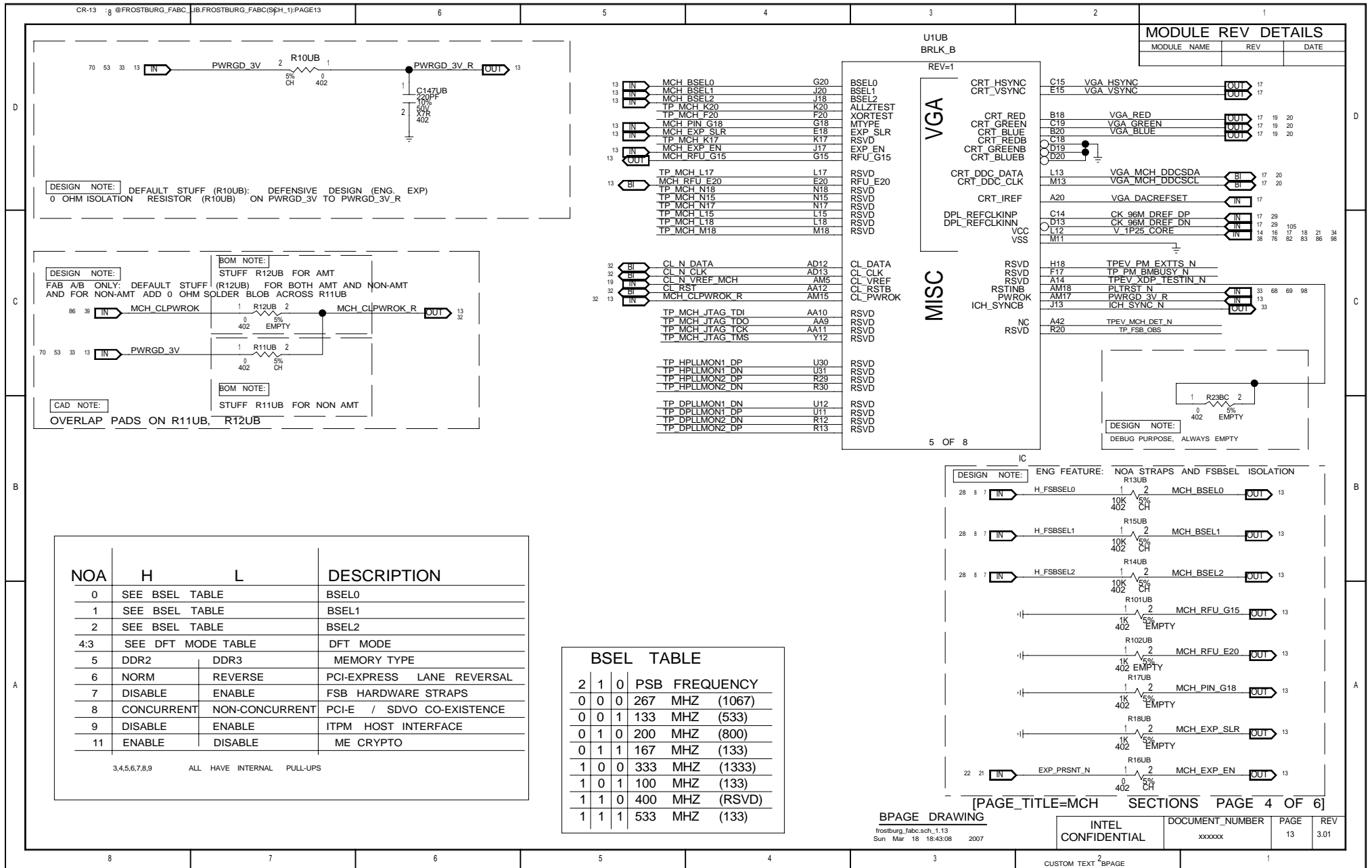


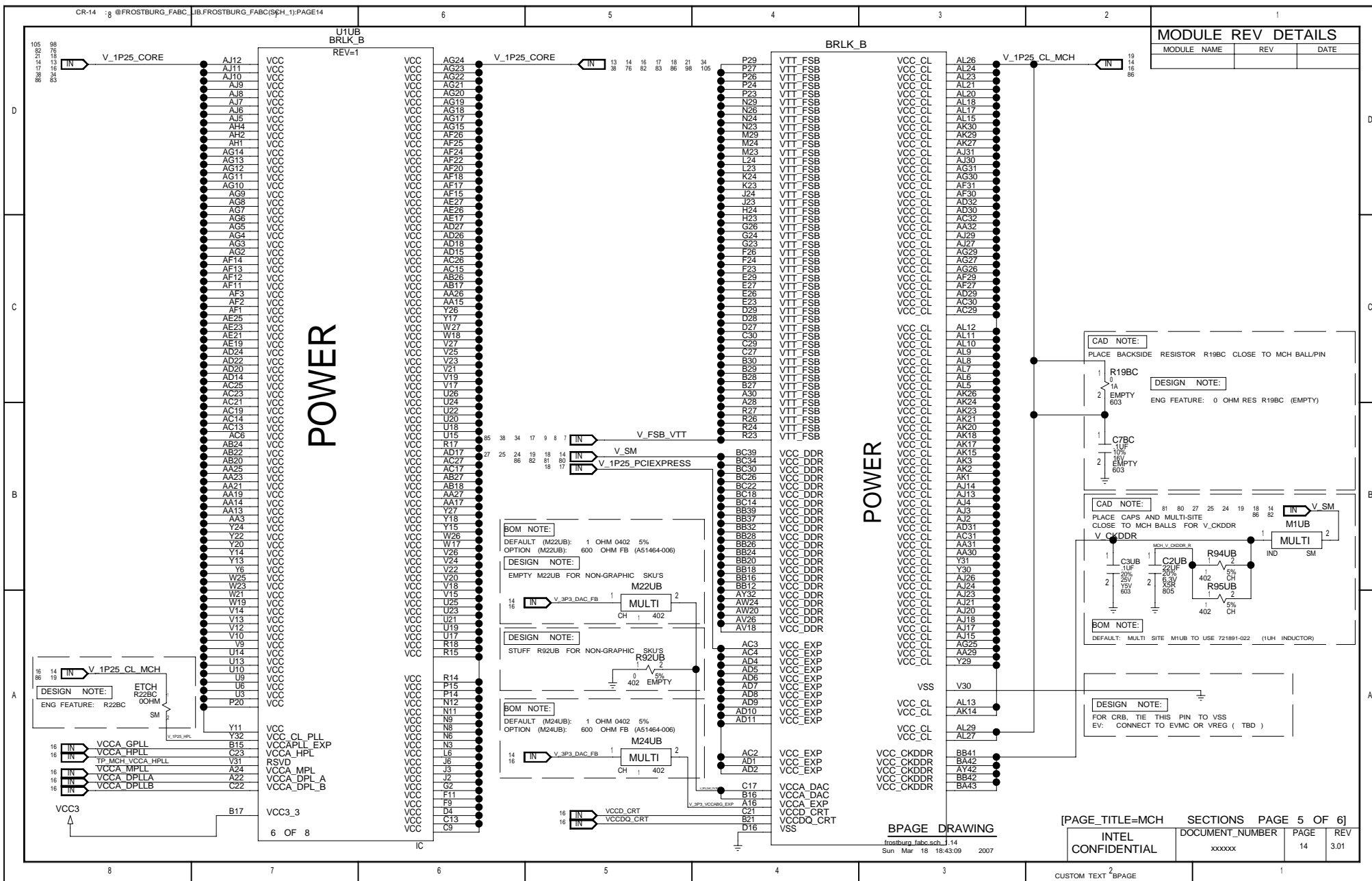


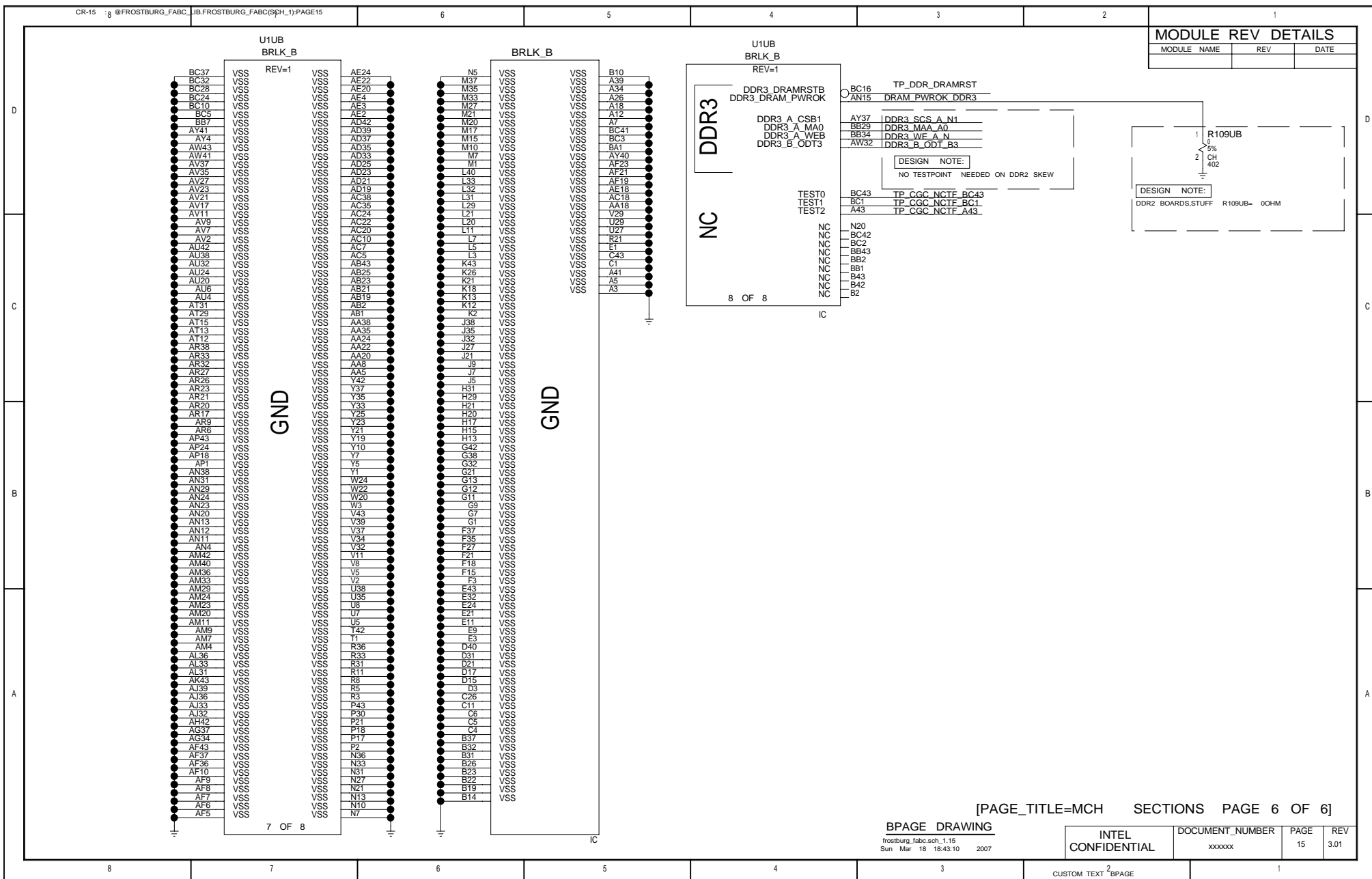


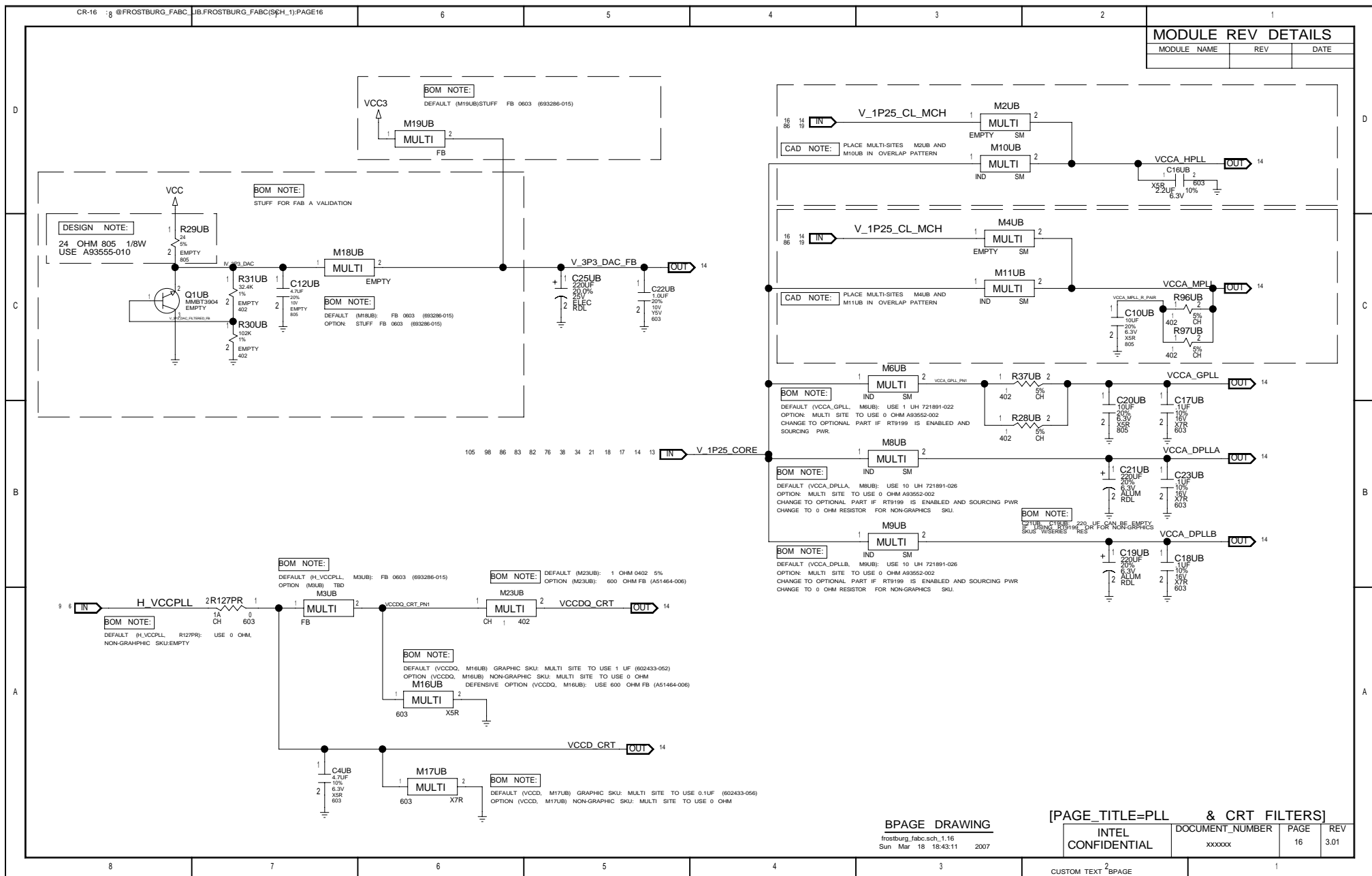


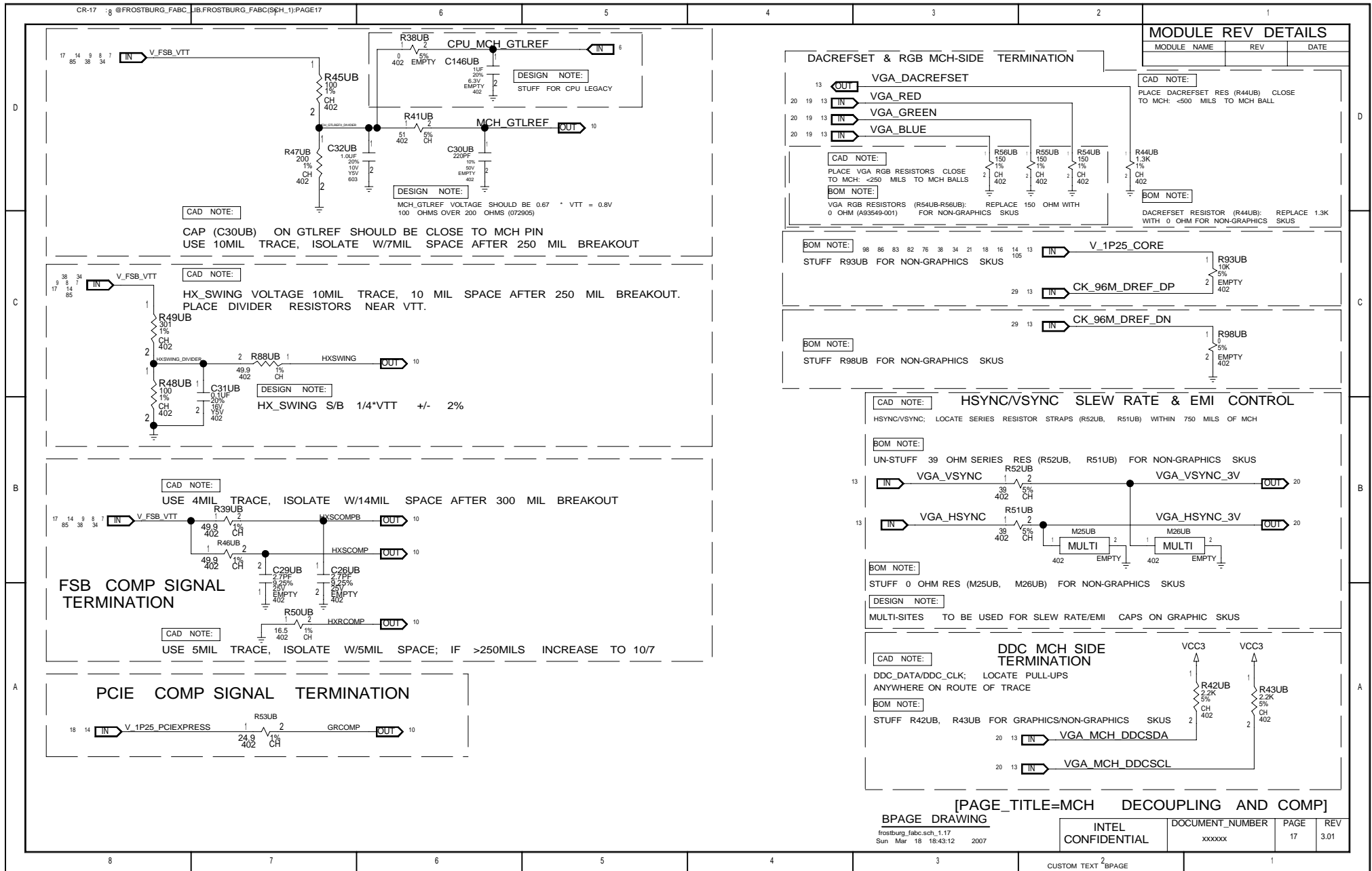


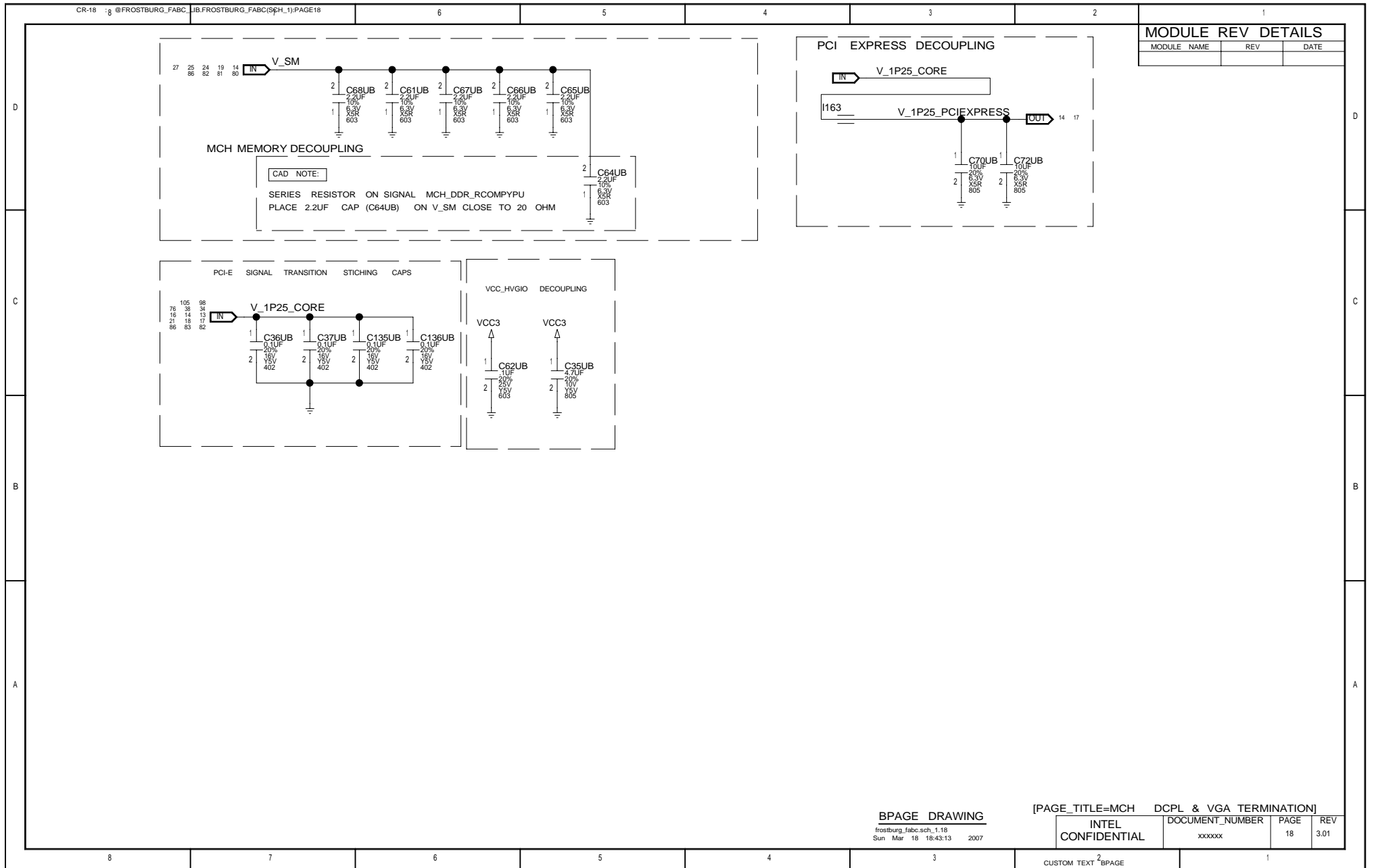


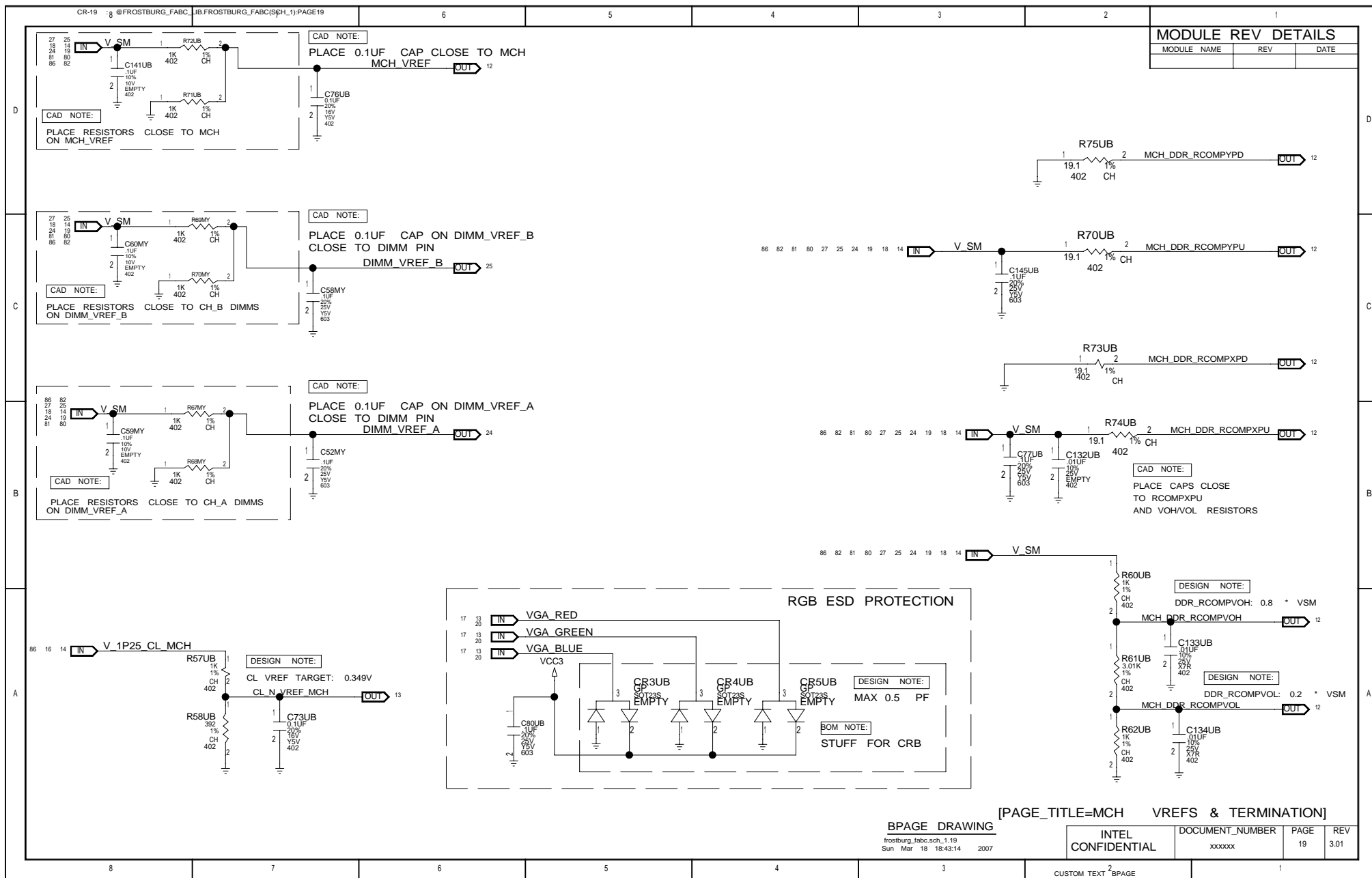


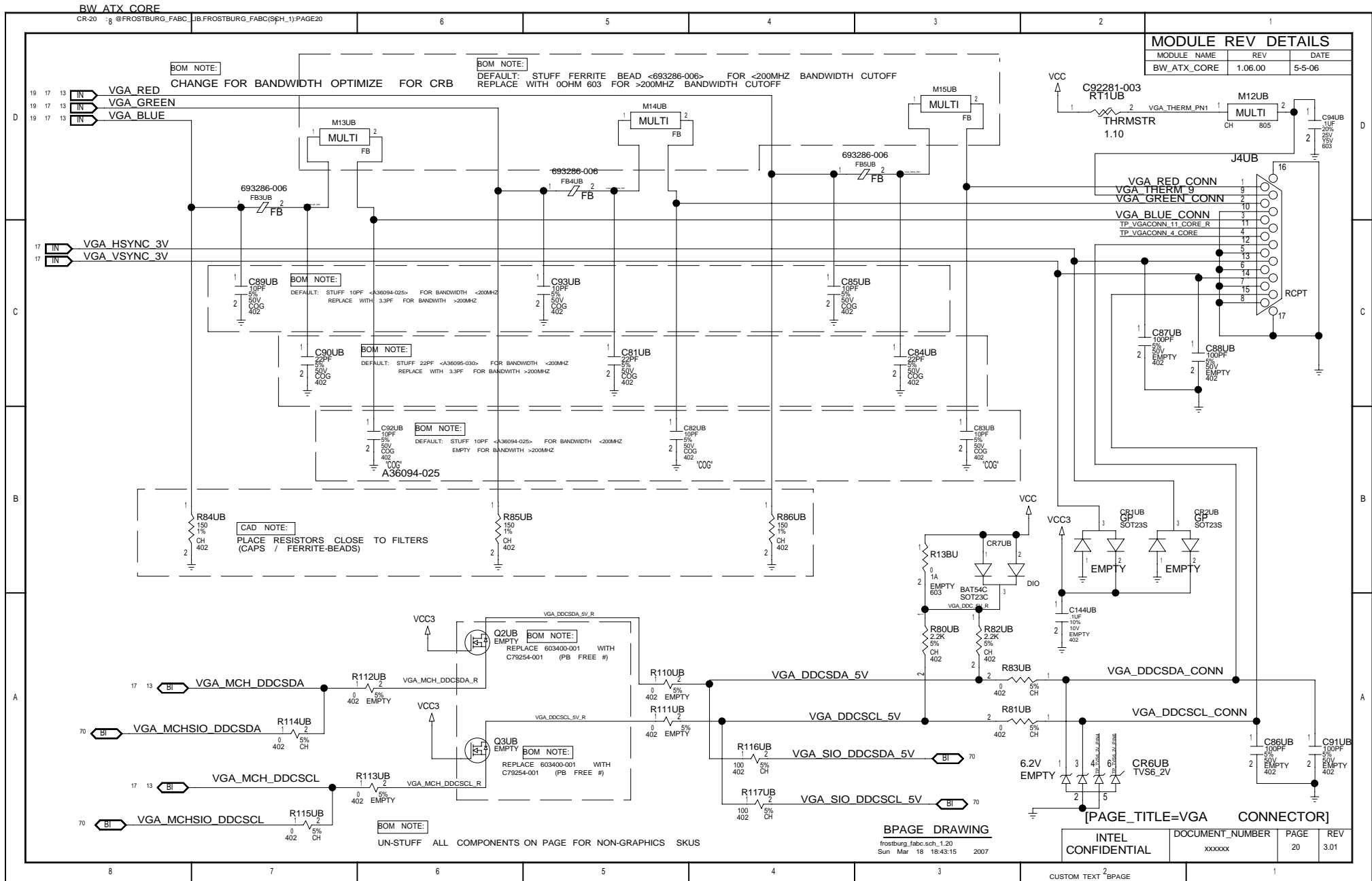












BW_ATX_CORE

CR-21 - 8 @FROSTBURG_FABC JB.FROSTBURG_FABC(Sch_1)-PAGE21

SLOT 1

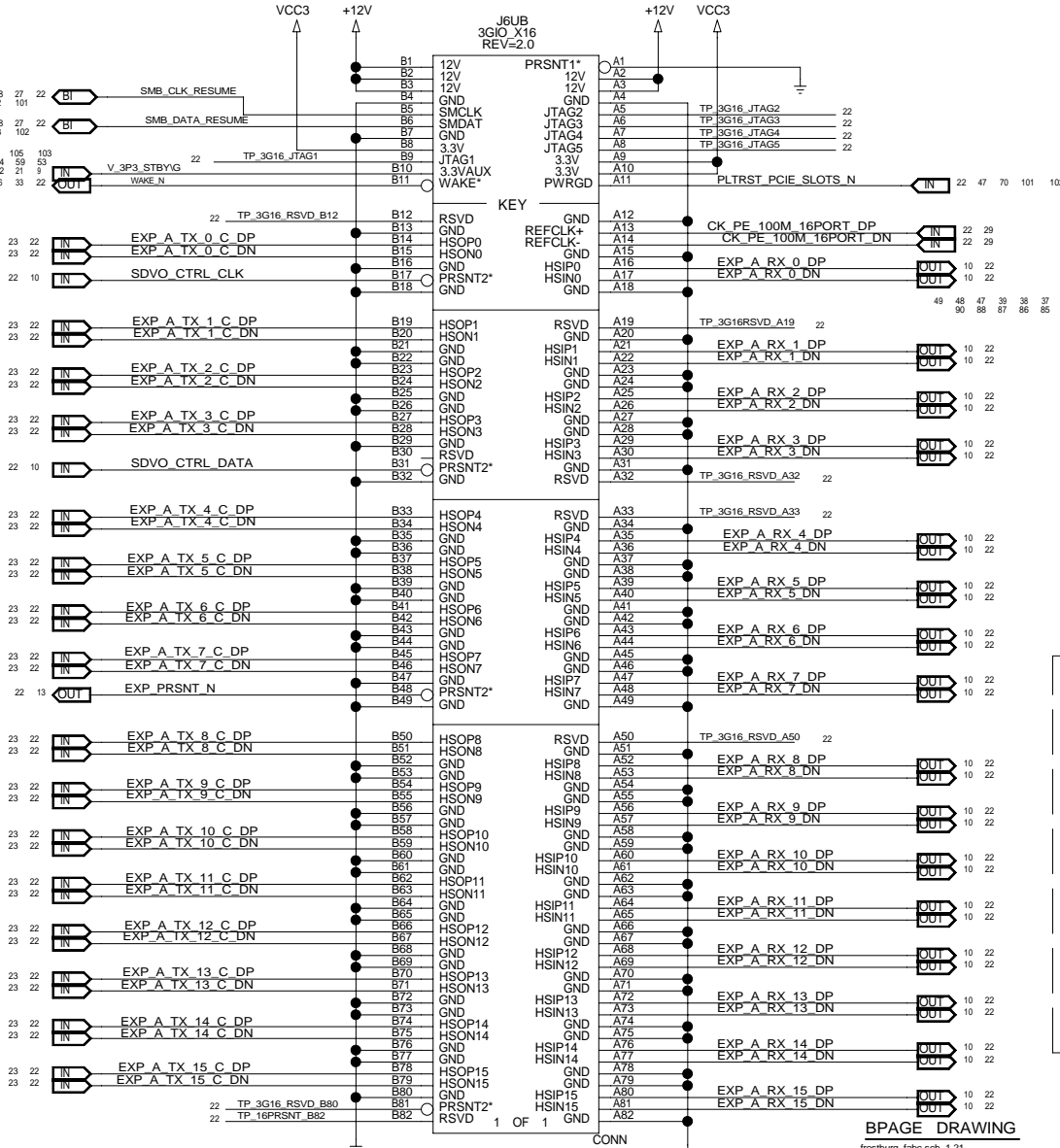
PCI EXPRESS
16-PORT
RIGHT LATCH
(DEFAULT)

BOM NOTE:

STUFF J6UB

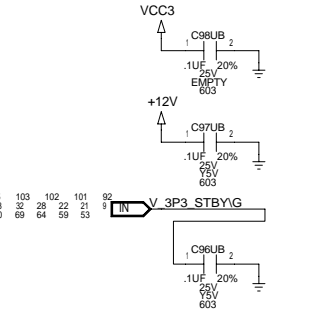
EMPTY J10UB

88	87	86	85	84	82	70	68	64	59	53	105	103	101	102	101	92	90
38	36	37	36	34	33	32	28	22	21	9	102	101	98	47	36	33	32

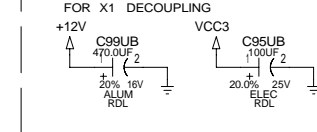


MODULE REV DETAILS

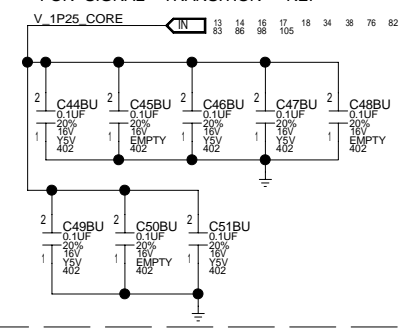
MODULE NAME	REV	DATE
BW_ATX_CORE	1.06.00	5-5-06



DESIGN NOTE:
ALWAYS STUFF C99UB & C95UB
EVEN IF J6UB IS EMPTY
FOR X1 DECOUPLING



CAD NOTE:
PLACE NEAR EDGE OF PEG SLOT
FOR SIGNAL TRANSITION REF



[PAGE_TITLE=PCI EXPRESS X16]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	xxxxxxx	21	3.01

BPAGE DRAWING
frostburg_fabc.sch_1.21
Sun Mar 18 18:43:16 2007

CUSTOM TEXT BPAGE

BW_ATX_CORE

CR-22 -g @FROSTBURG_FABC JB.FROSTBURG_FABC(Sch_1)-PAGE22

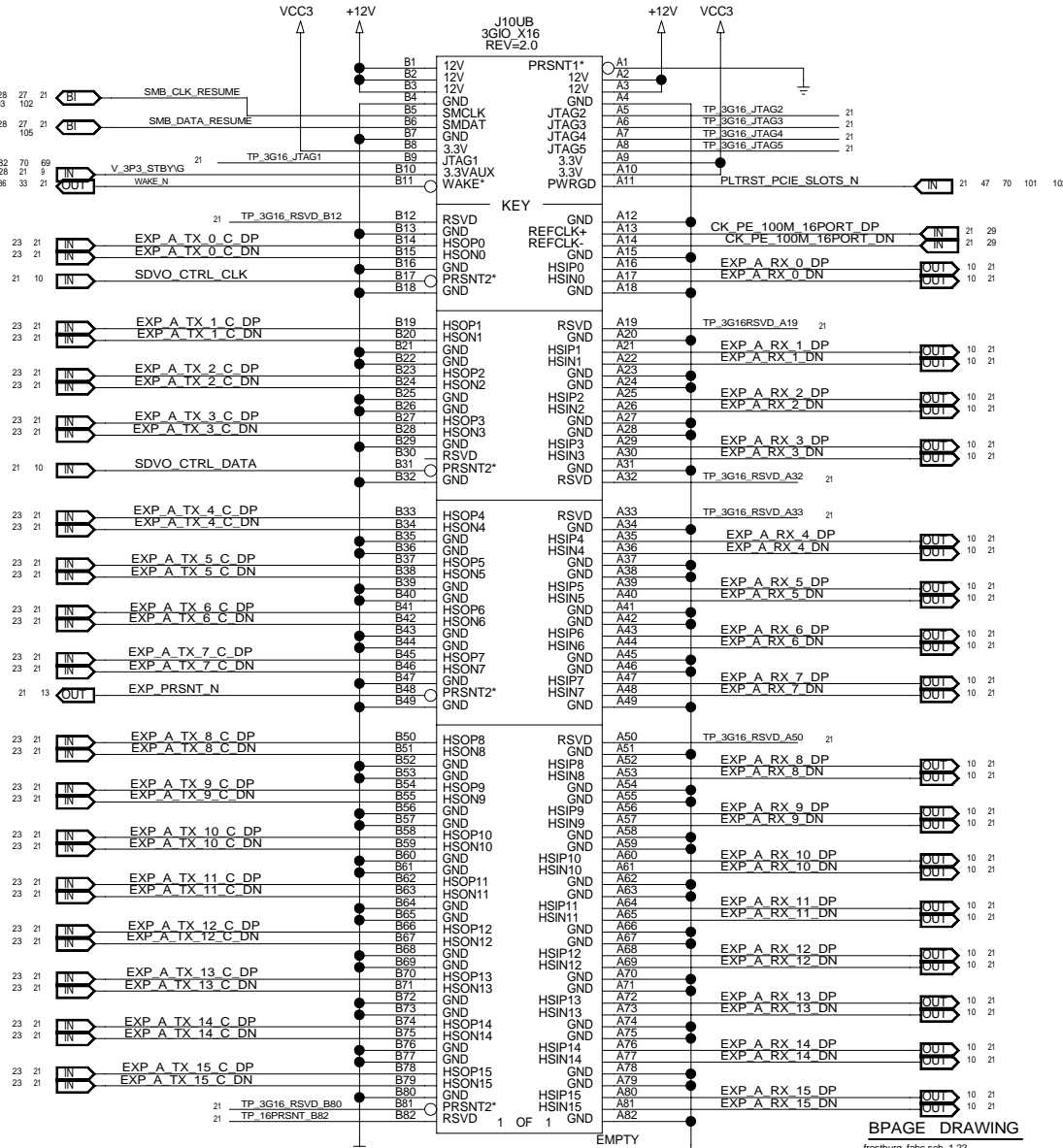
SLOT 1

PCI EXPRESS
16-PORT
LEFT LATCH

BOM NOTE:

STUFF J6UB
EMPTY J10UB

64 59 53 49 48 47 33 28 27 21 101 102 103 105 90 88 87 86 85 84 82 70 69 47 38 37 36 34 33 32 28 21 101 102 103 105



DESIGN NOTE:

PCI E X16 GRAPHIC CONNECTOR WITH LEFT LATCH

MODULE REV DETAILS

MODULE NAME	REV	DATE
BW_ATX_CORE	1.06.00	5-5-06

[PAGE_TITLE=PCI EXPRESS X16]

INTEL CONFIDENTIAL	DOCUMENT NUMBER xxxxxxx	PAGE 22	REV 3.01
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BPAGE DRAWING

frostburg_fabc.sch_1.22
Sun Mar 18 18:43:17 2007

CUSTOM TEXT BPAGE

BW ATX CORE

CR-23 : 8 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(SCH_1):PAGE23

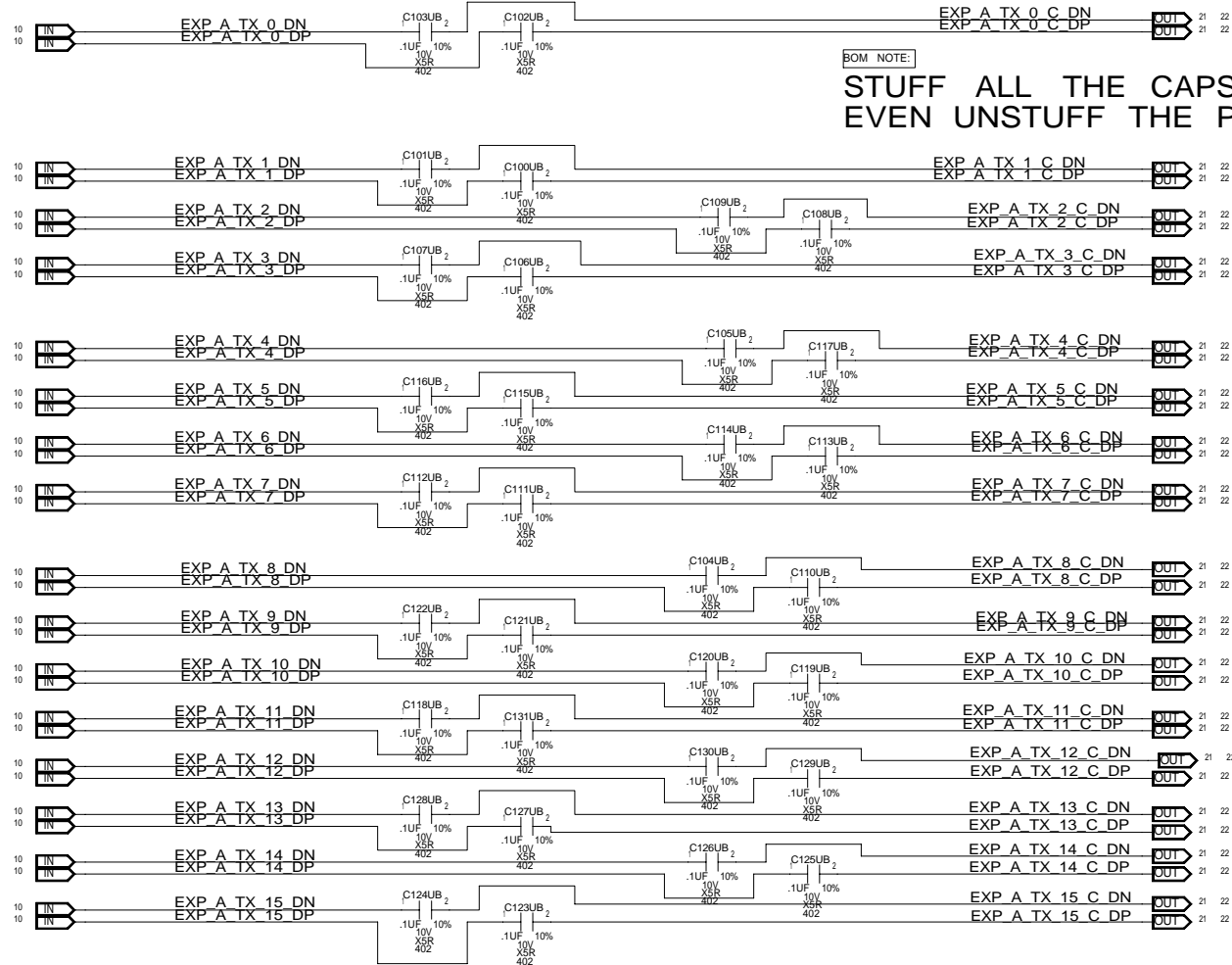
6

5

4

1

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BW_ATX_CORE	1.06.00	5-5-06



BOM NOTE:

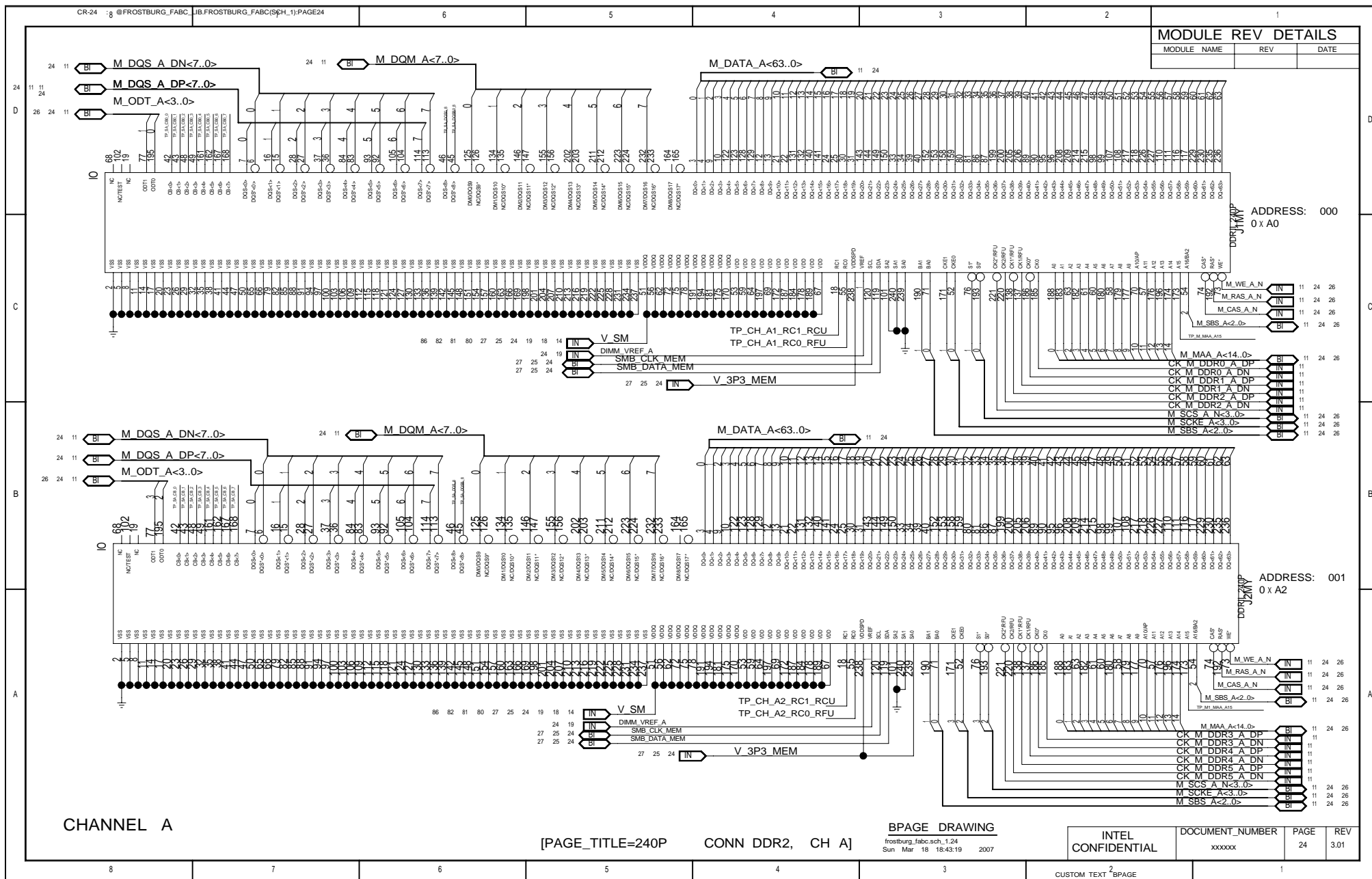
STUFF ALL THE CAPS
EVEN UNSTUFF THE PCIEX16

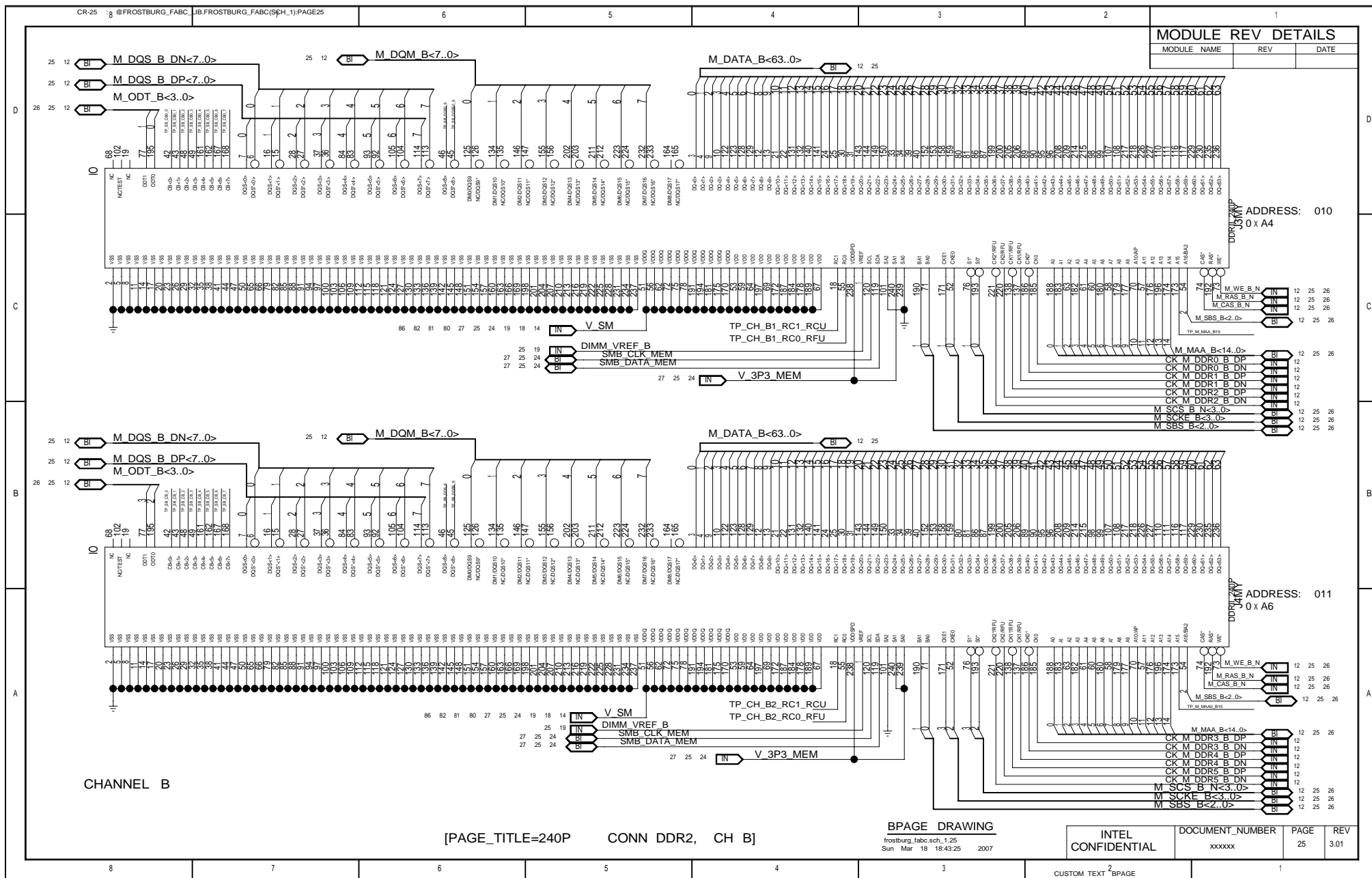
[PAGE_TITLE=PCI EXPRESS X16 COUPLING]

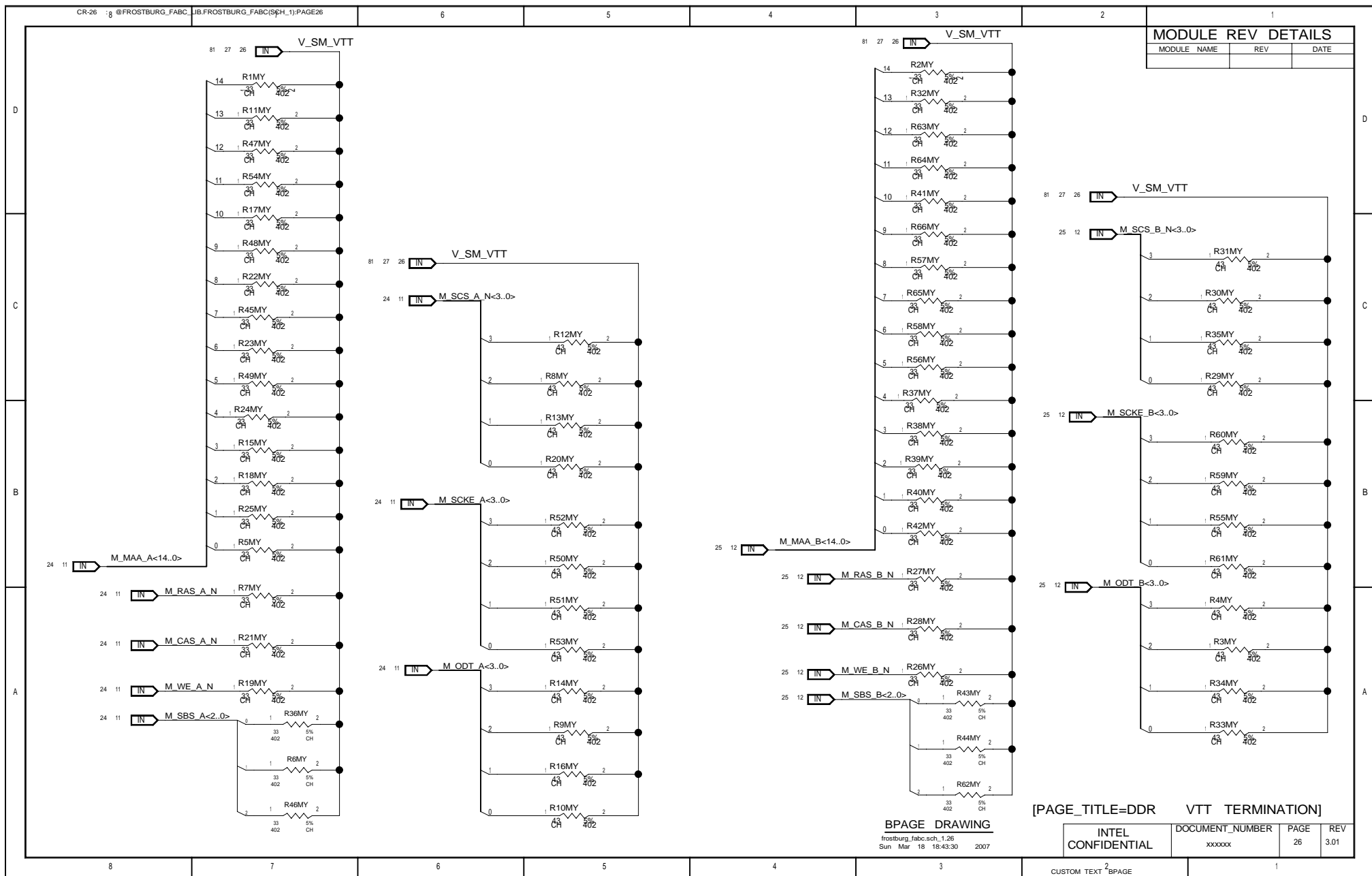
BPAGE DRAWING
frostburg_fabc.sch_1.23
Sun Mar 18 18:43:18 2007

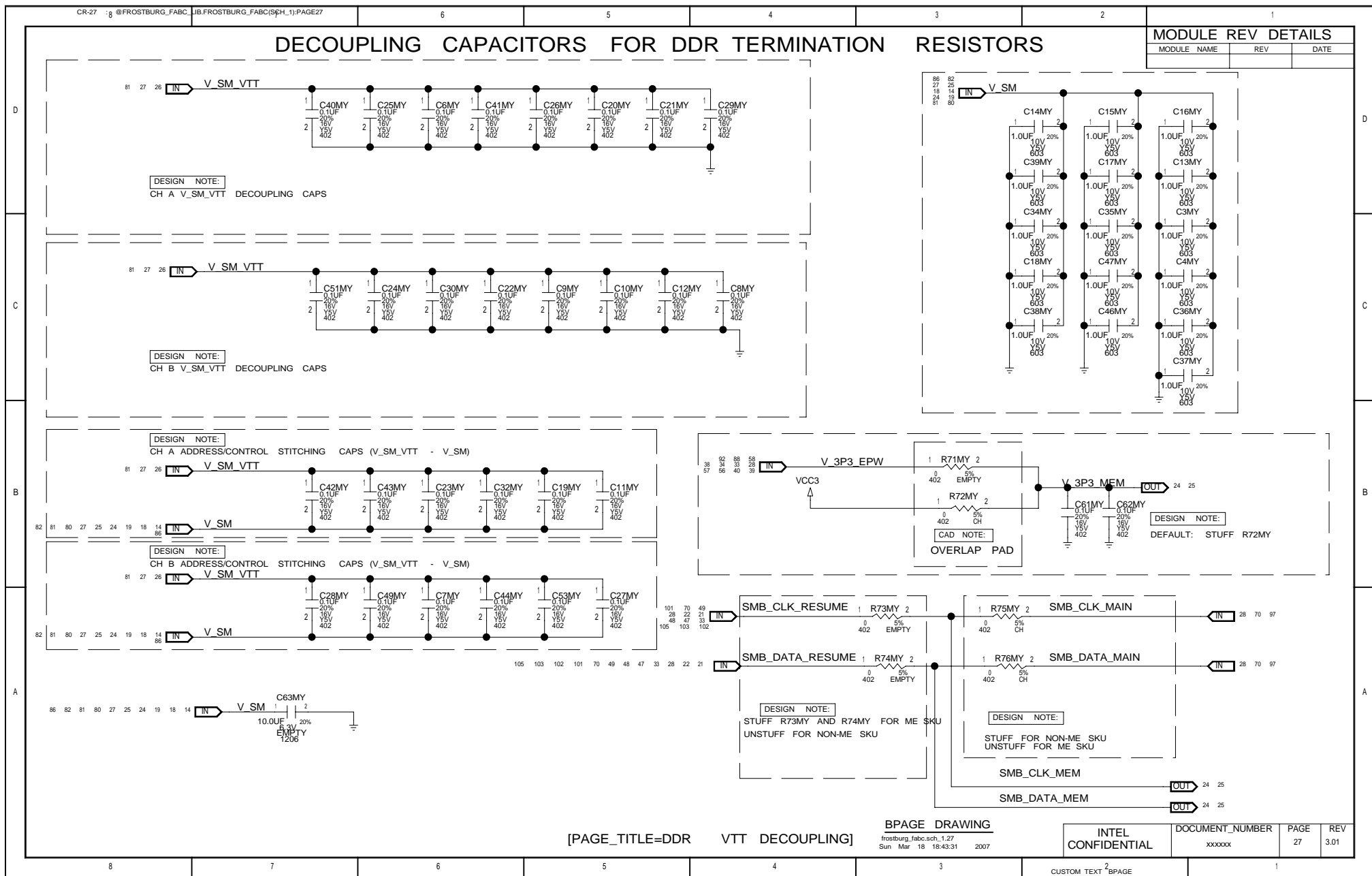
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxx	PAGE 23	REV 3.01
-----------------------	---------------------------	------------	-------------

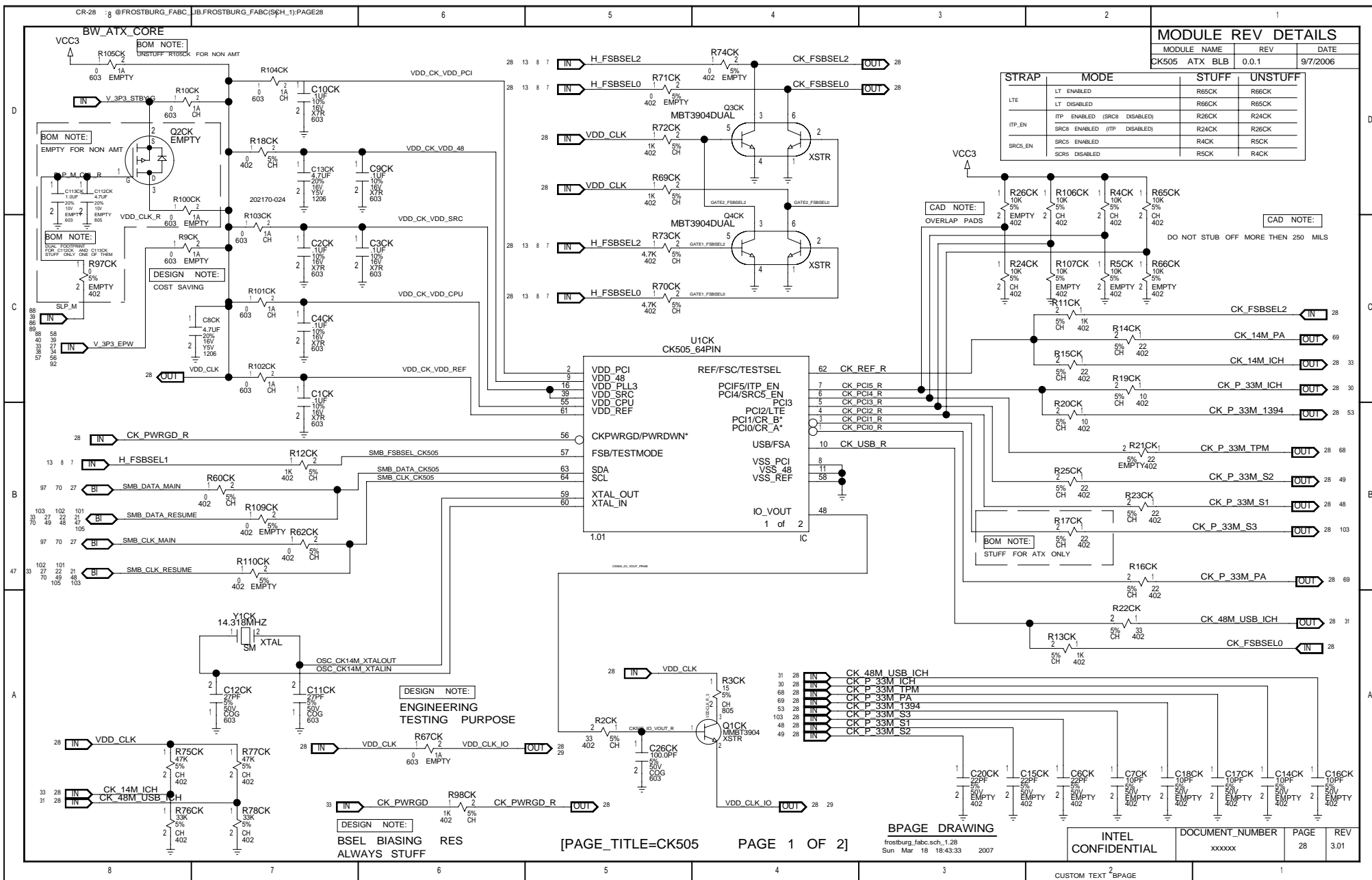
CUSTOM TEXT²BPAGE











BW ATX CORE

CR-29 -g @FROSTBURG_FABC JB.FROSTBURG_FABC(SqH_1)-PAGE29

MODULE REV DETAILS

MODULE NAME	REV	DATE
CK505 ATX BLB	0.0.1	9-7-2006

CAD NOTE: CK505 VDD_1JO BULK DCPL: PLACE AROUND CK505

DESIGN NOTE:
STUFF C104CK AND C110CK
FOR 64 PINS

CAD NOTE: CK505 VDD_1JO DCPL: PLACE (1) PER PIN

U1CK
CK505_64PIN

1.01

2 of 2

IC

12

20

26

45

49

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51

53

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15

19

23

42

52

29

VDD IO

VDD PLL3 IO

VDD SRC IO

VDD CPU IO

VDD SRC IO

SRC8-/ITP-

SRC8+/ITP+

CPU1-

CPU1+

CPU0-

CPU0+

VSS IO

VSS PLL3

VSS SRC

VSS CPU

VSS SRC

SRC7-/CR E-

SRC7+/CR F+

SRC6-

SRC6+

CPU_STOP-/SRC5-

CPU_STOP+/SRC5+

SRC4-

SRC4+

SRC3-/CR D-

SRC3+/CR C+

SRC2-/SATA-

SRC2+/SATA+

SRC1-/SE2

SRC1+/SE1

SRC0-/DOT96-

SRC0+/DOT96+

BPAGE DRAWING

frostburg_fabc.sch_1.29
Sun Mar 18 18:43:34 2007

INTEL
CONFIDENTIAL

DOCUMENT NUMBER
xxxxxxx

PAGE
29

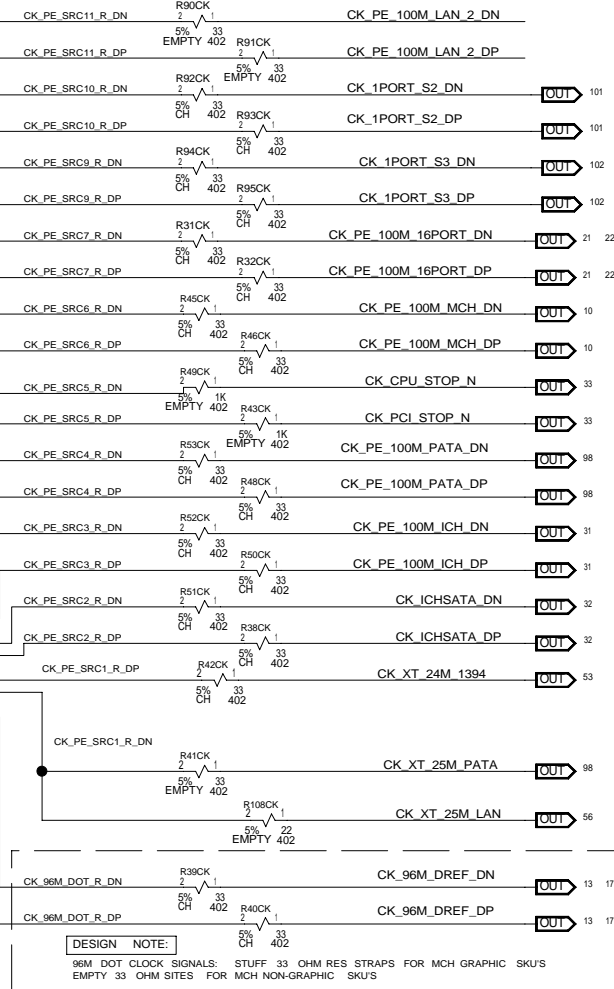
REV
3.01

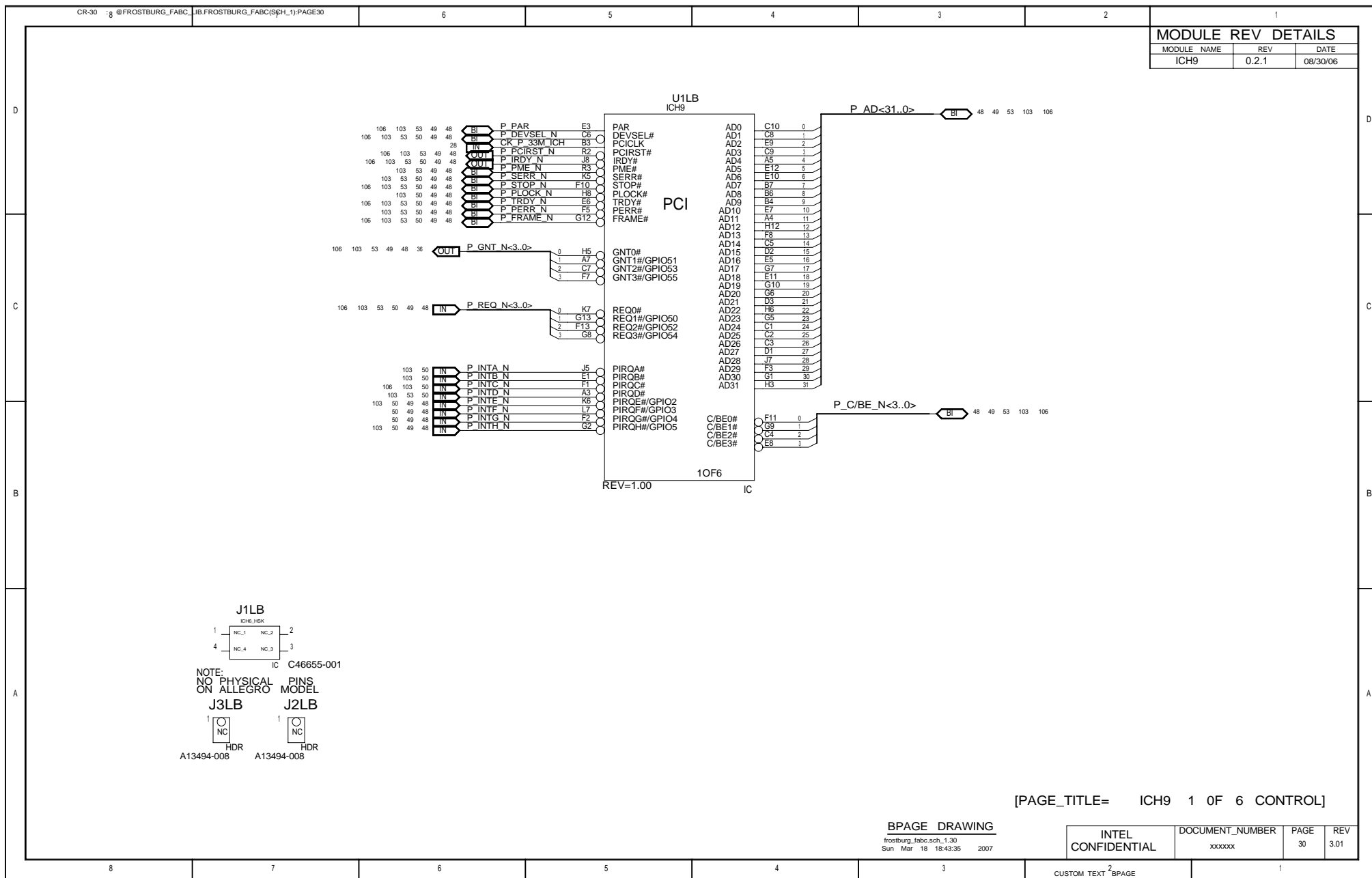
CUSTOM TEXT BPAGE

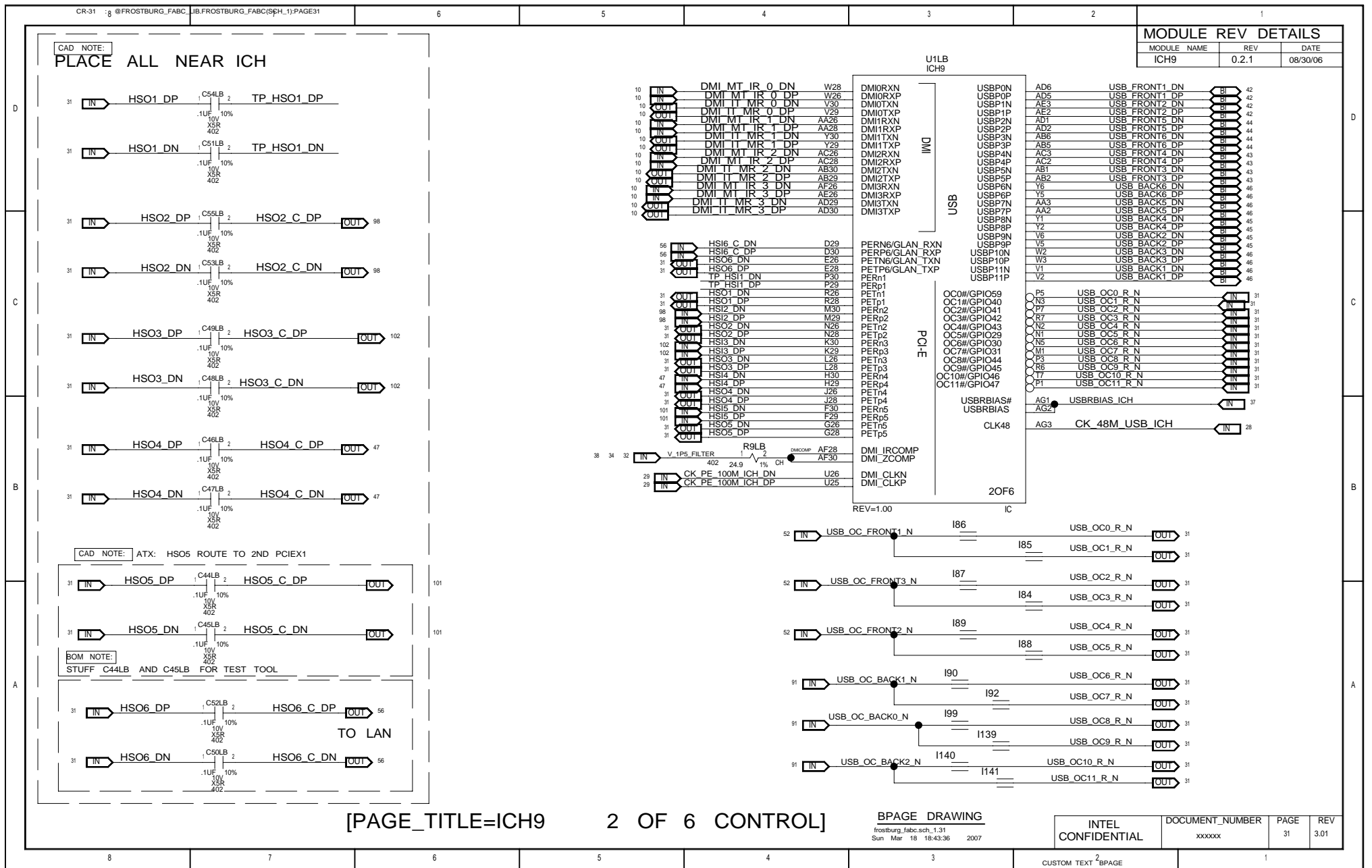
1

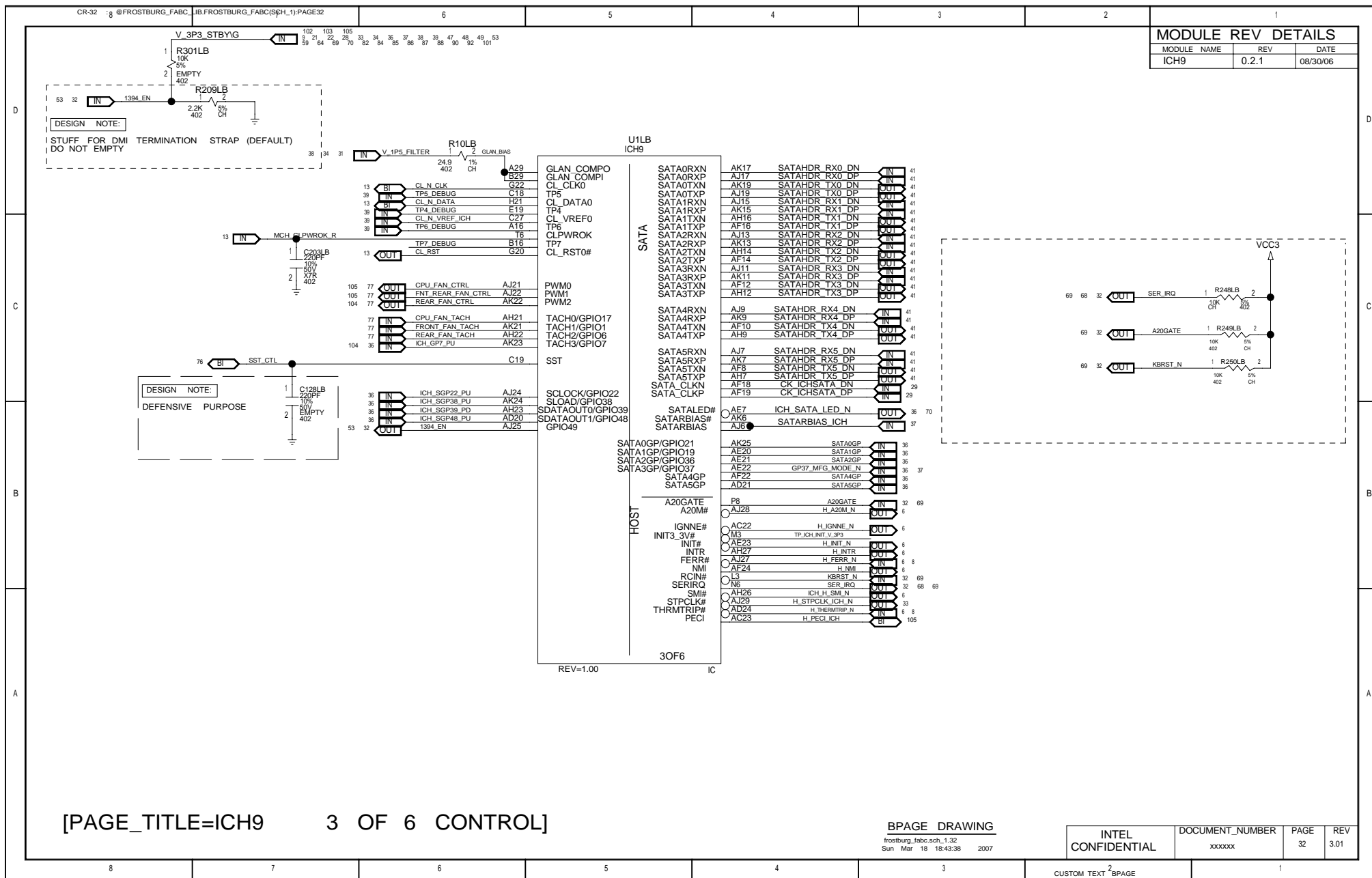
[PAGE_TITLE=CK505 PAGE 2 OF 2]

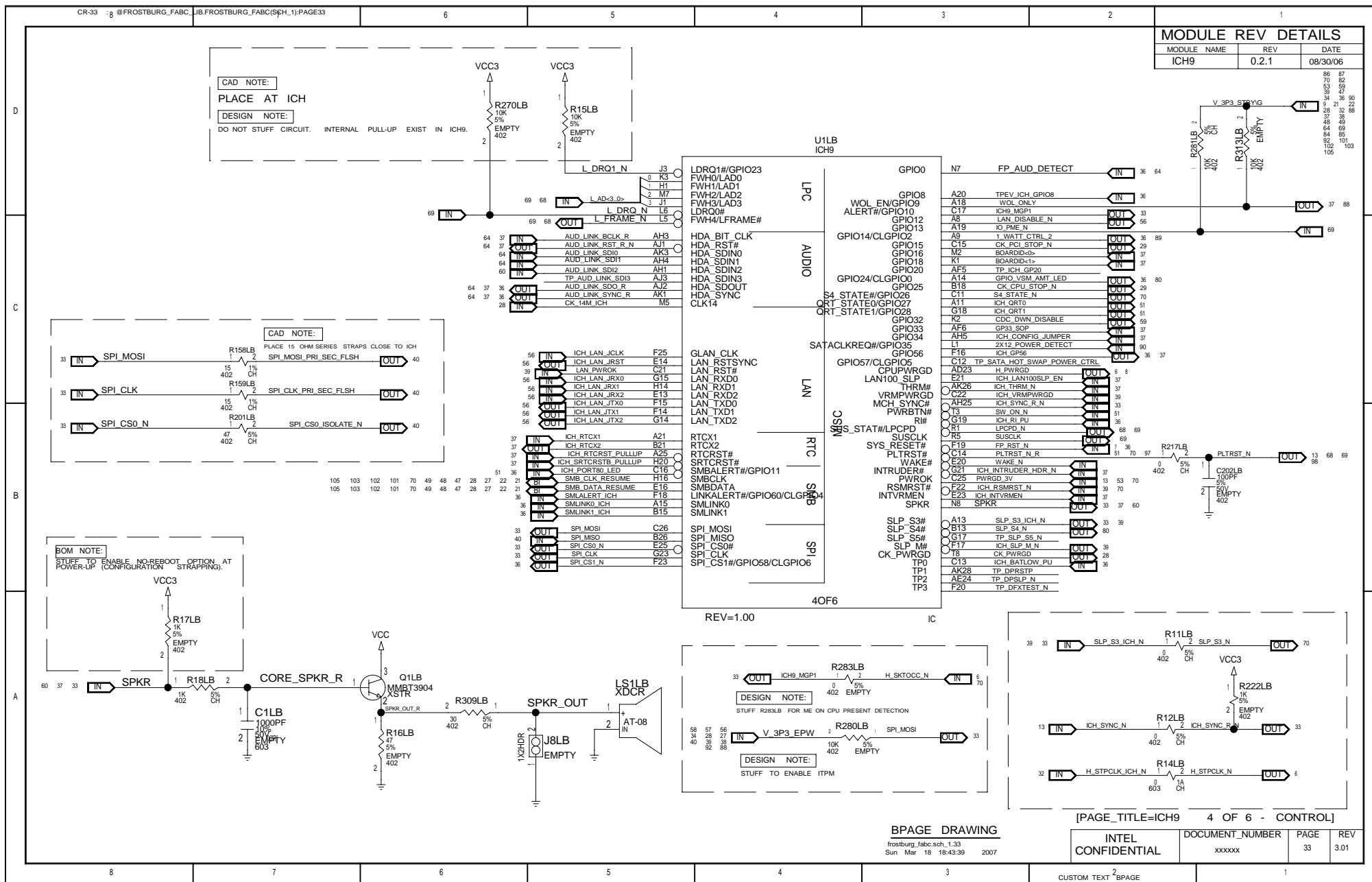
DESIGN NOTE:
96M DOT CLOCK SIGNALS: STUFF 33 OHM RES STRAPS FOR MCH GRAPHIC SKU'S
EMPTY 33 OHM SITES FOR MCH NON-GRAPHIC SKU'S

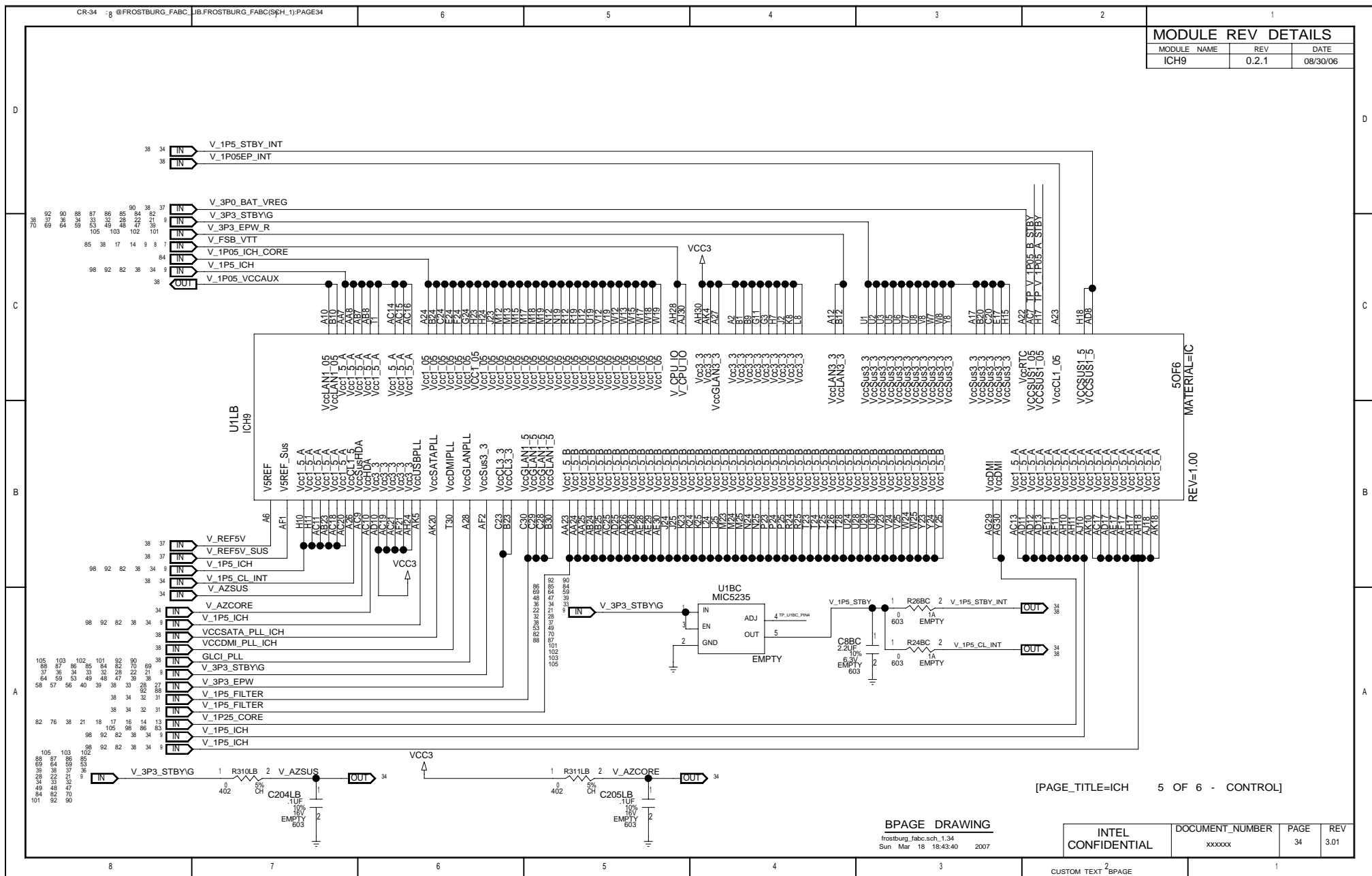




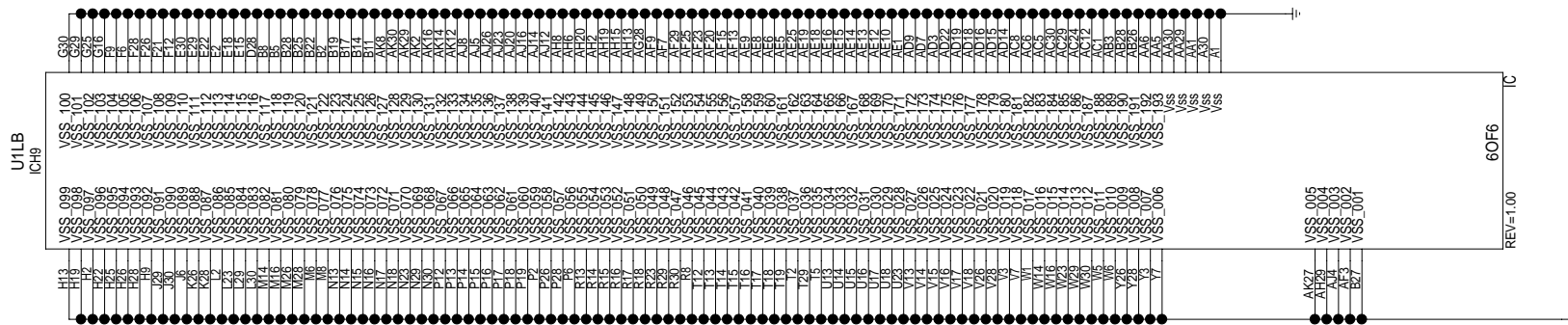








MODULE REV DETAILS			
MODULE	NAME	REV	DATE
ICH9		0.2.1	08/30/06



[PAGE_TITLE=ICH 6 OF 6 - GROUND BODY]

BPAGE DRAWING

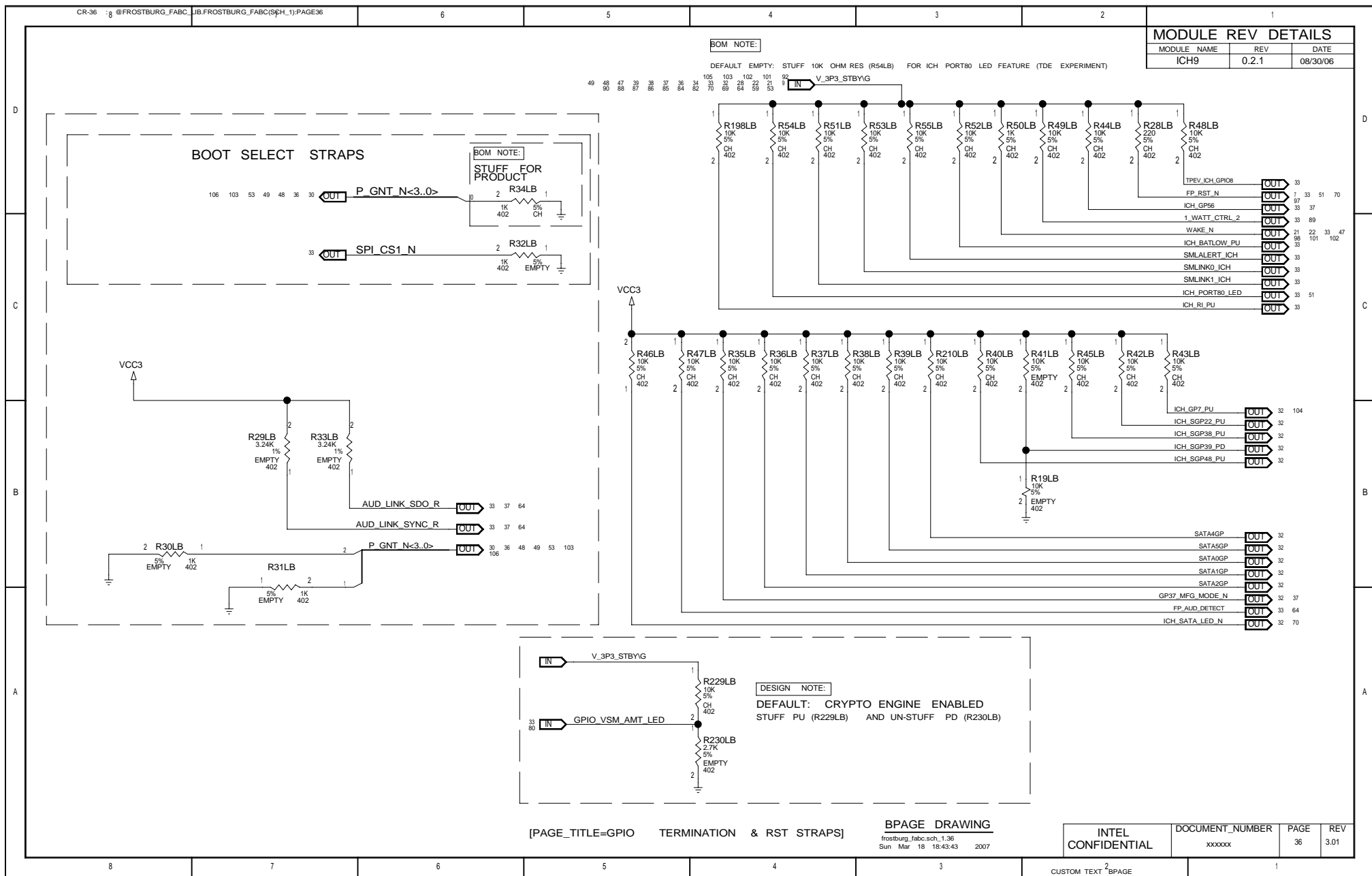
frostburg_fabc.sch_1.35
Sun Mar 18 18:43:41 2007

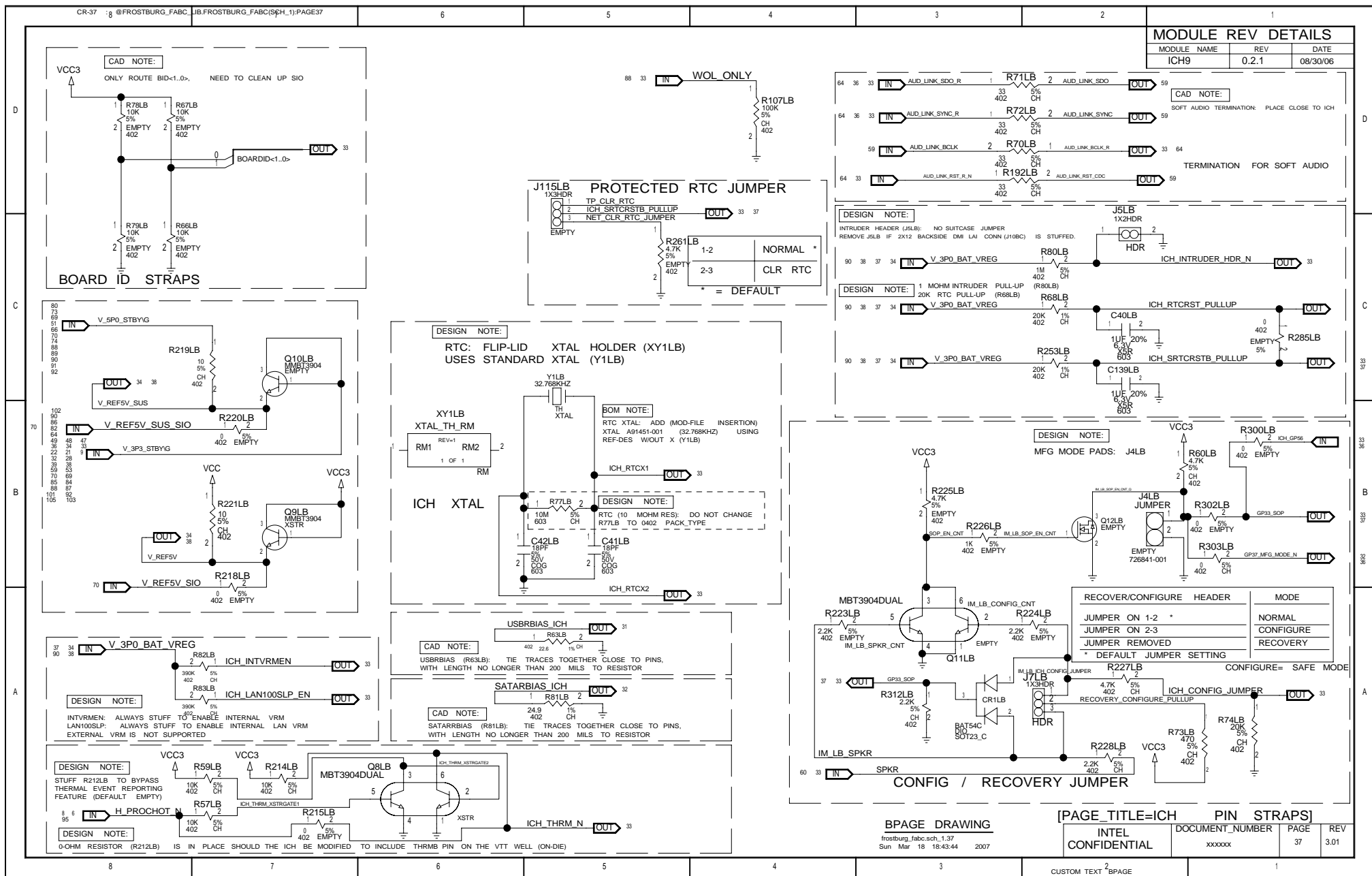
INTEL
CONFIDENTIAL

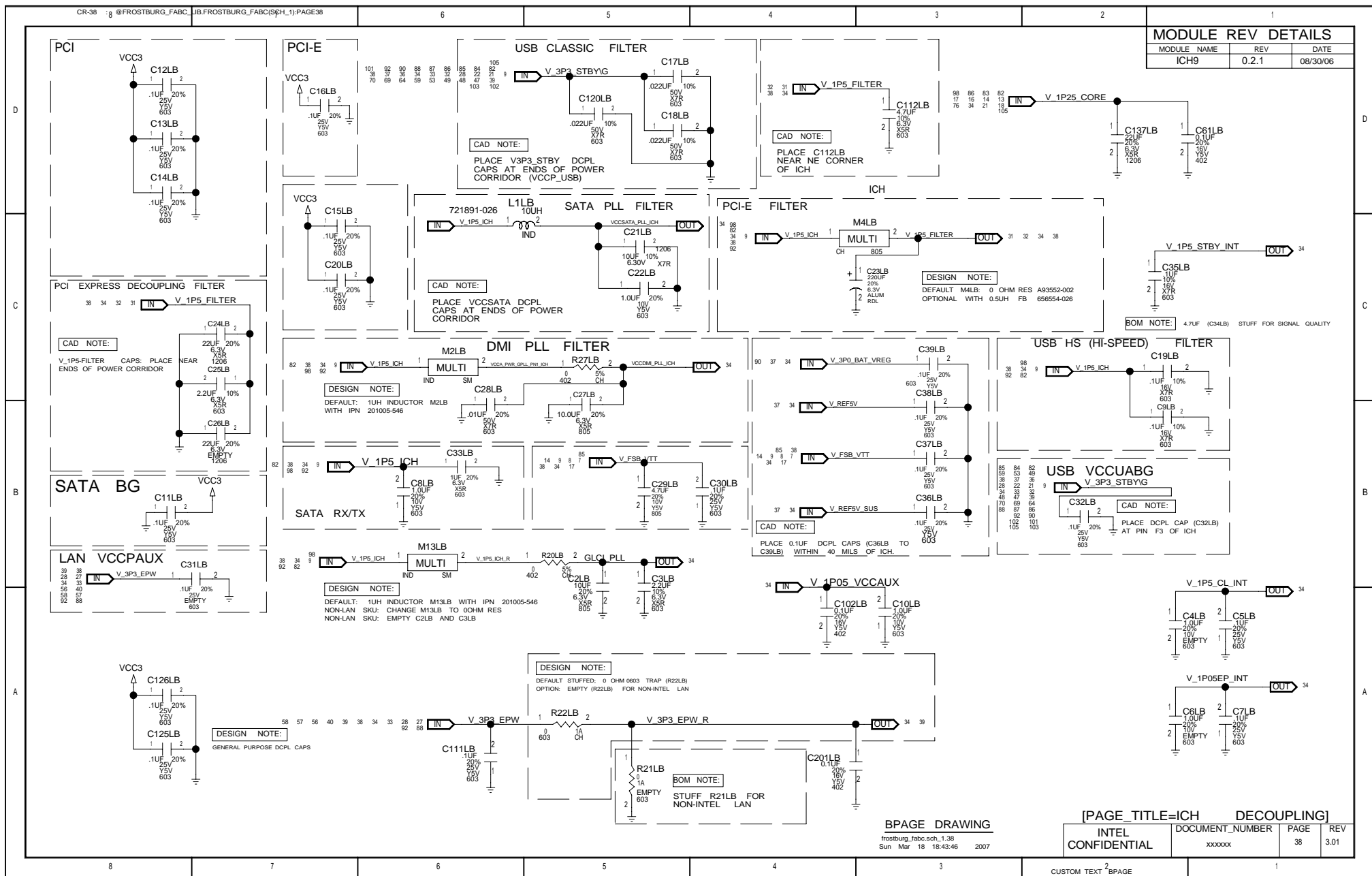
DOCUMENT_NUMBER
XXXXXX

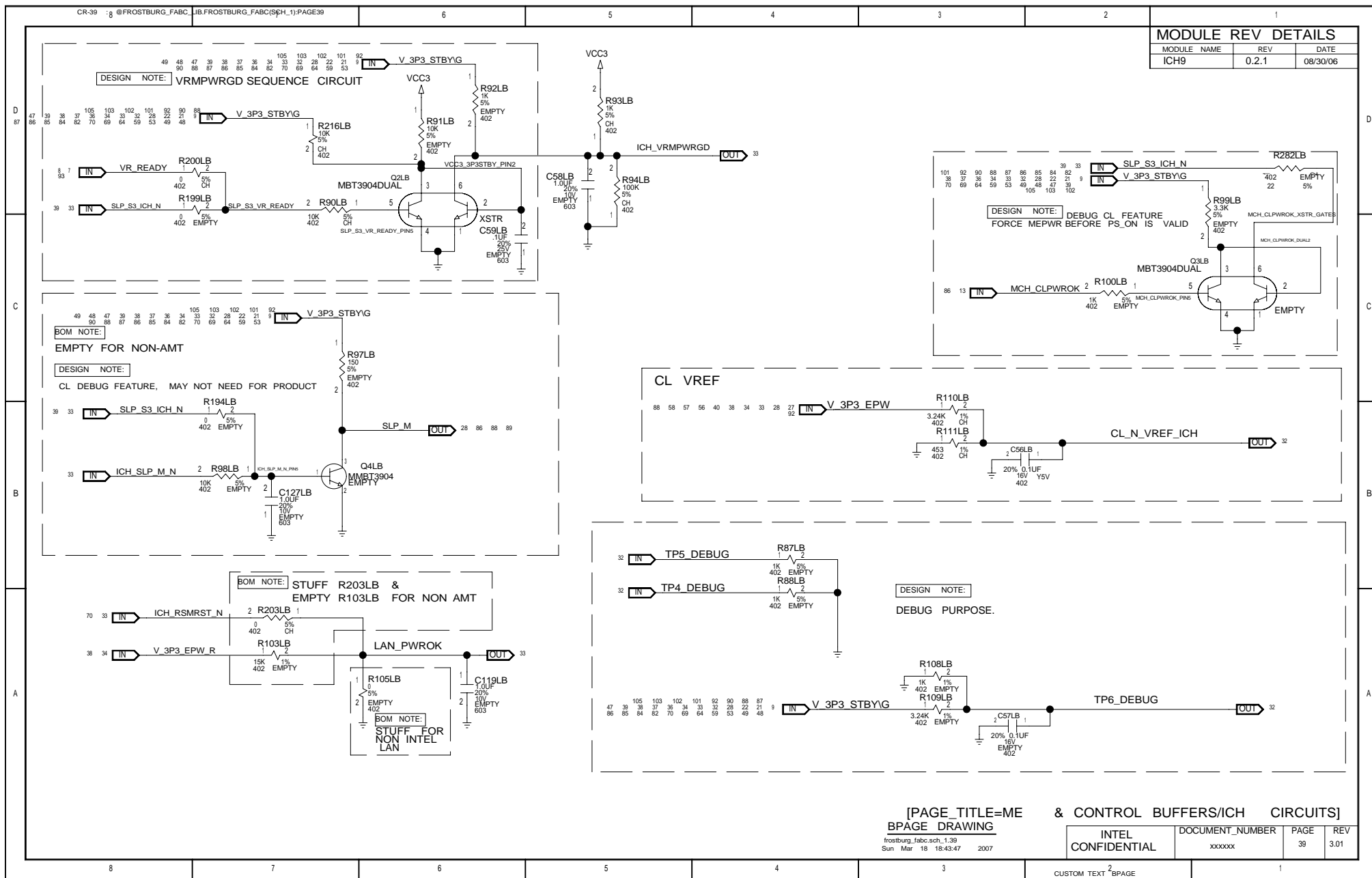
PAGE	REV
35	3.01

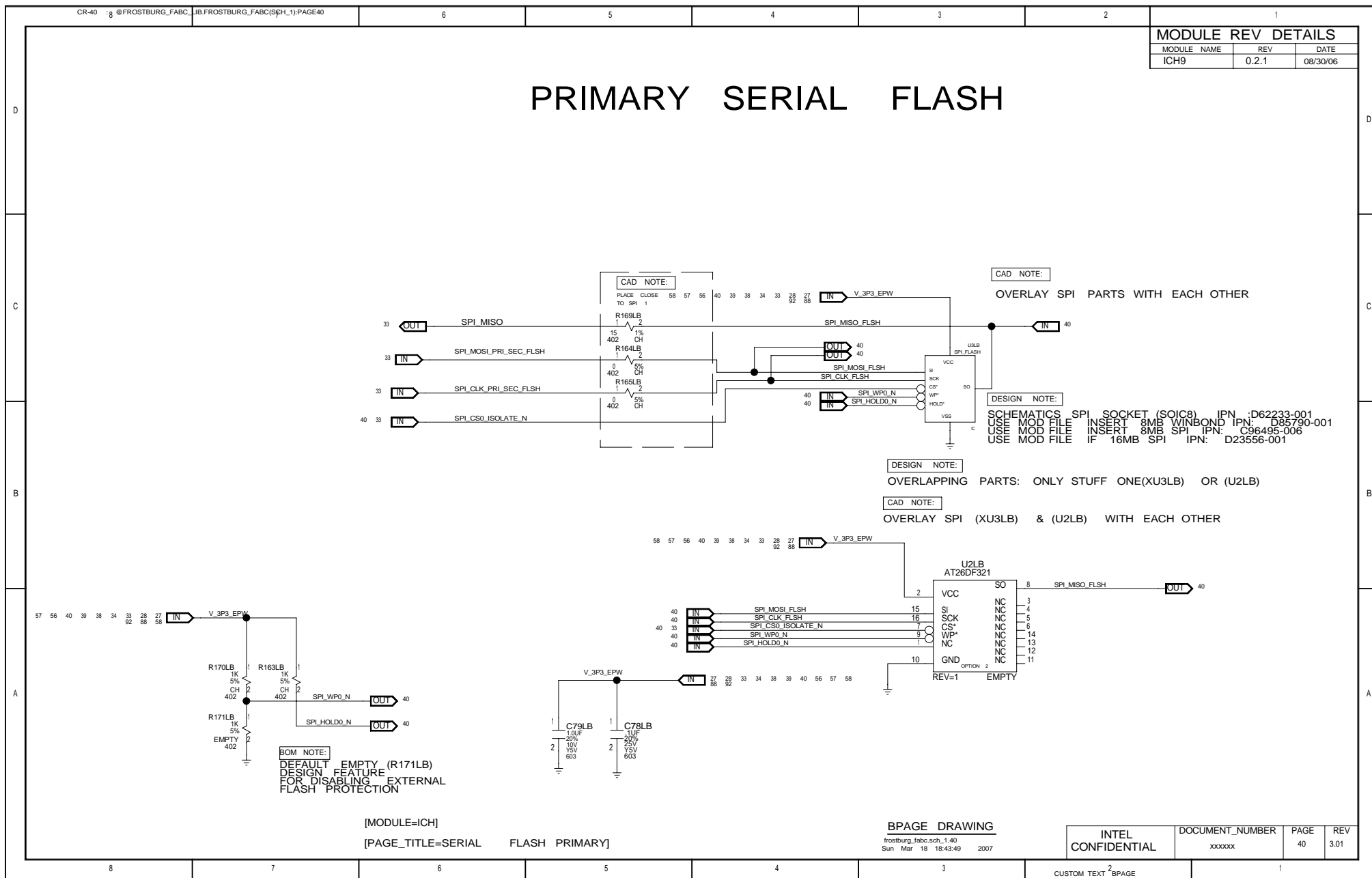
CUSTOM TEXT²BPAGE

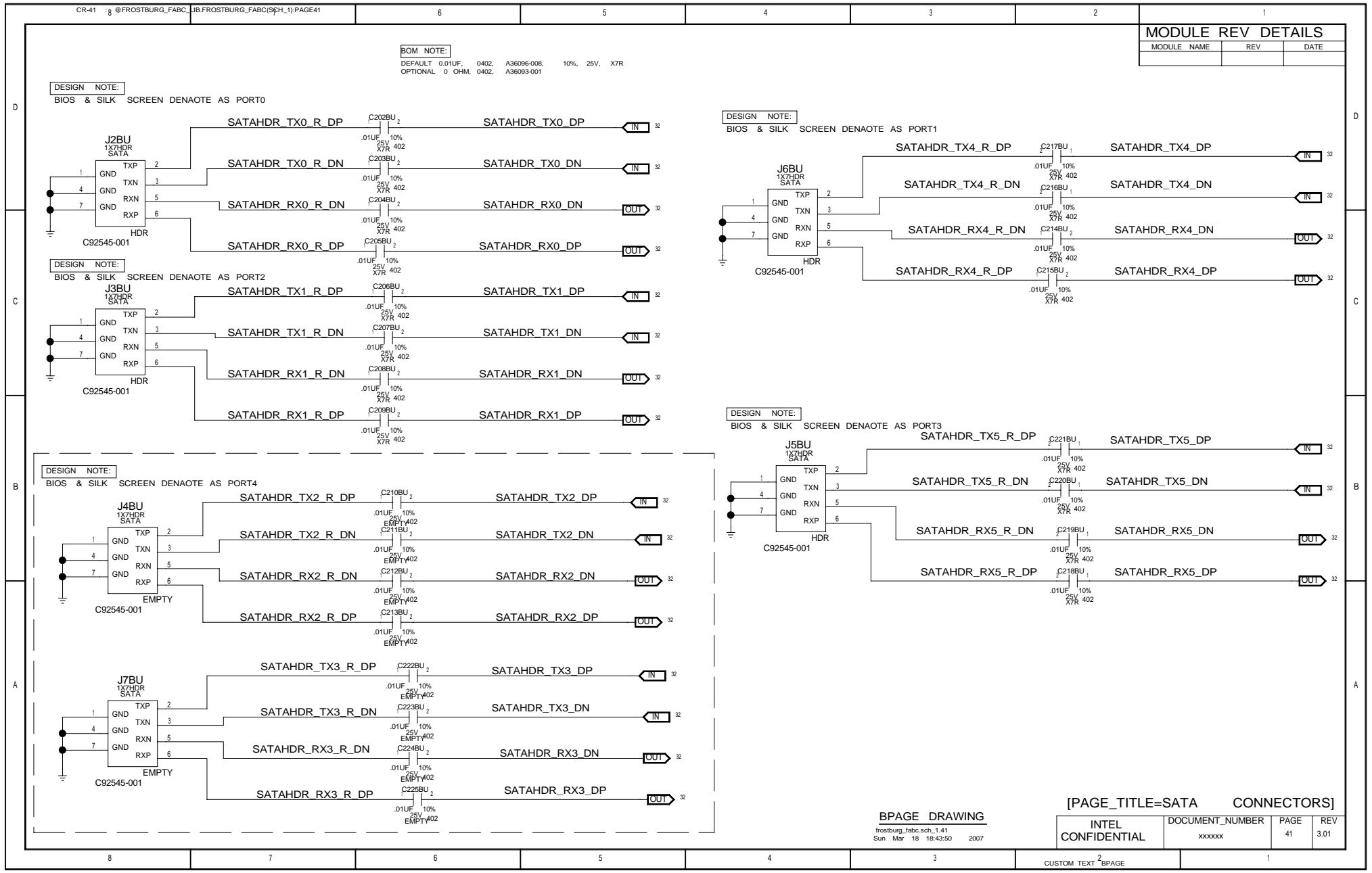


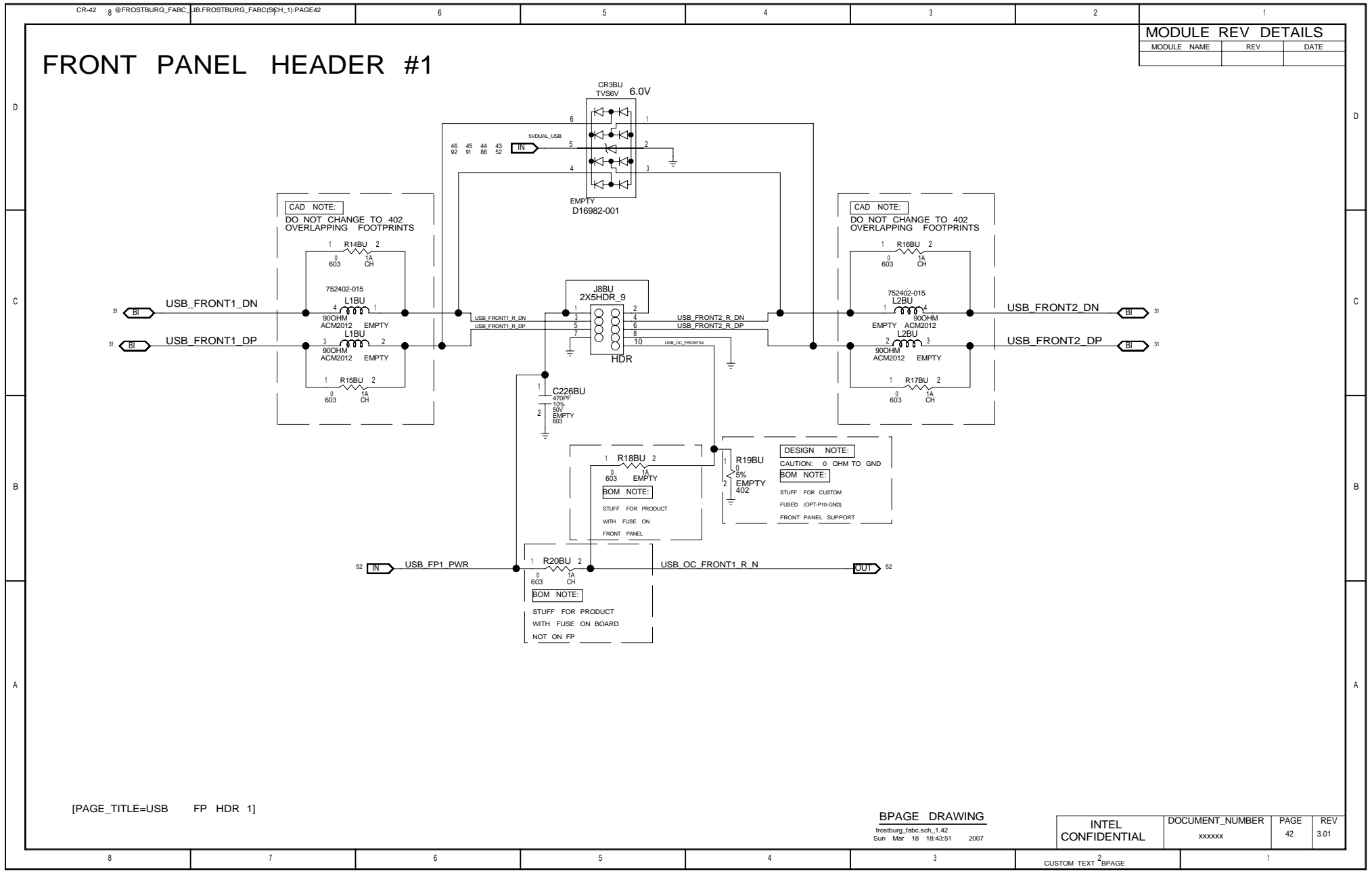


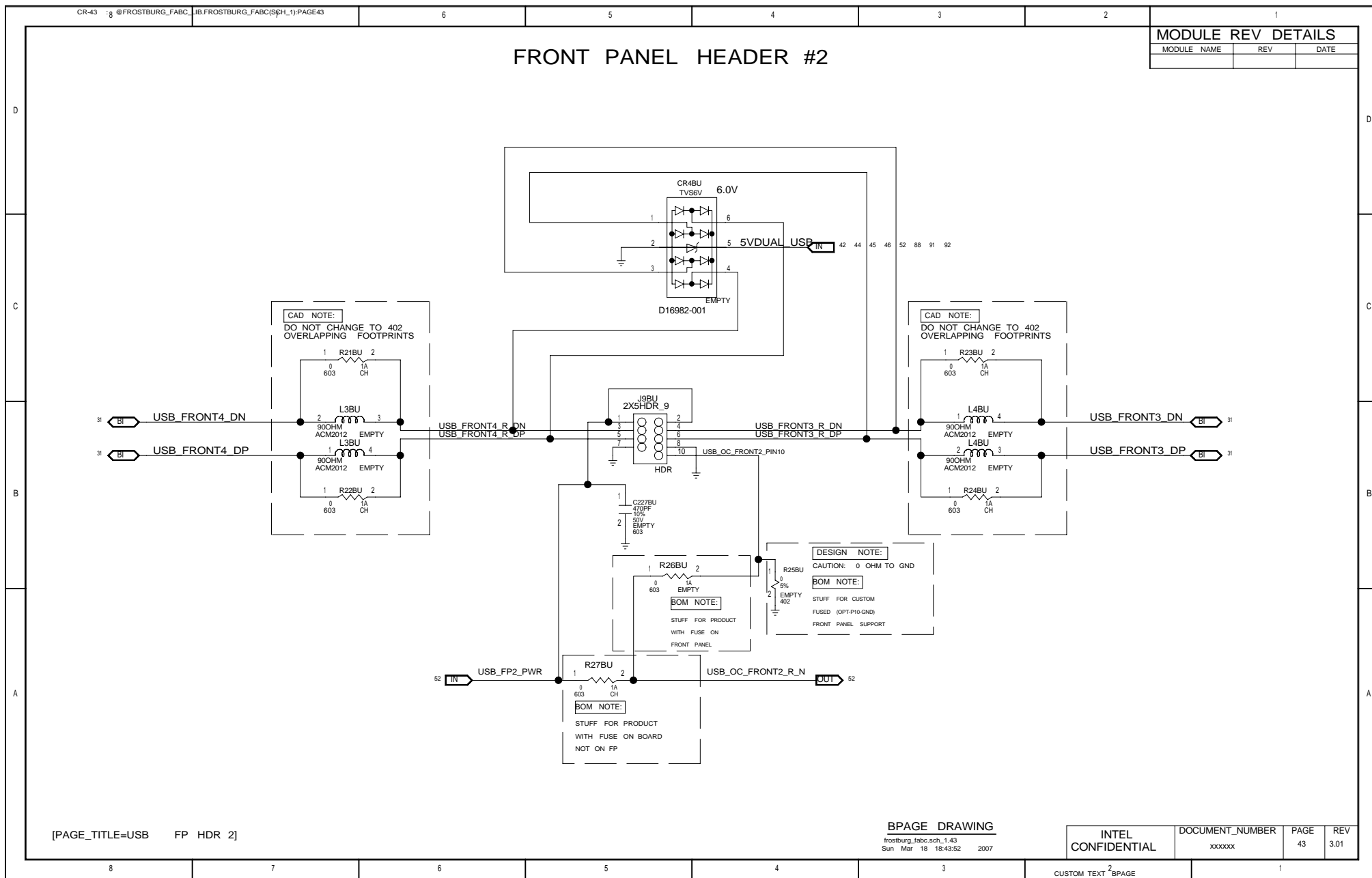


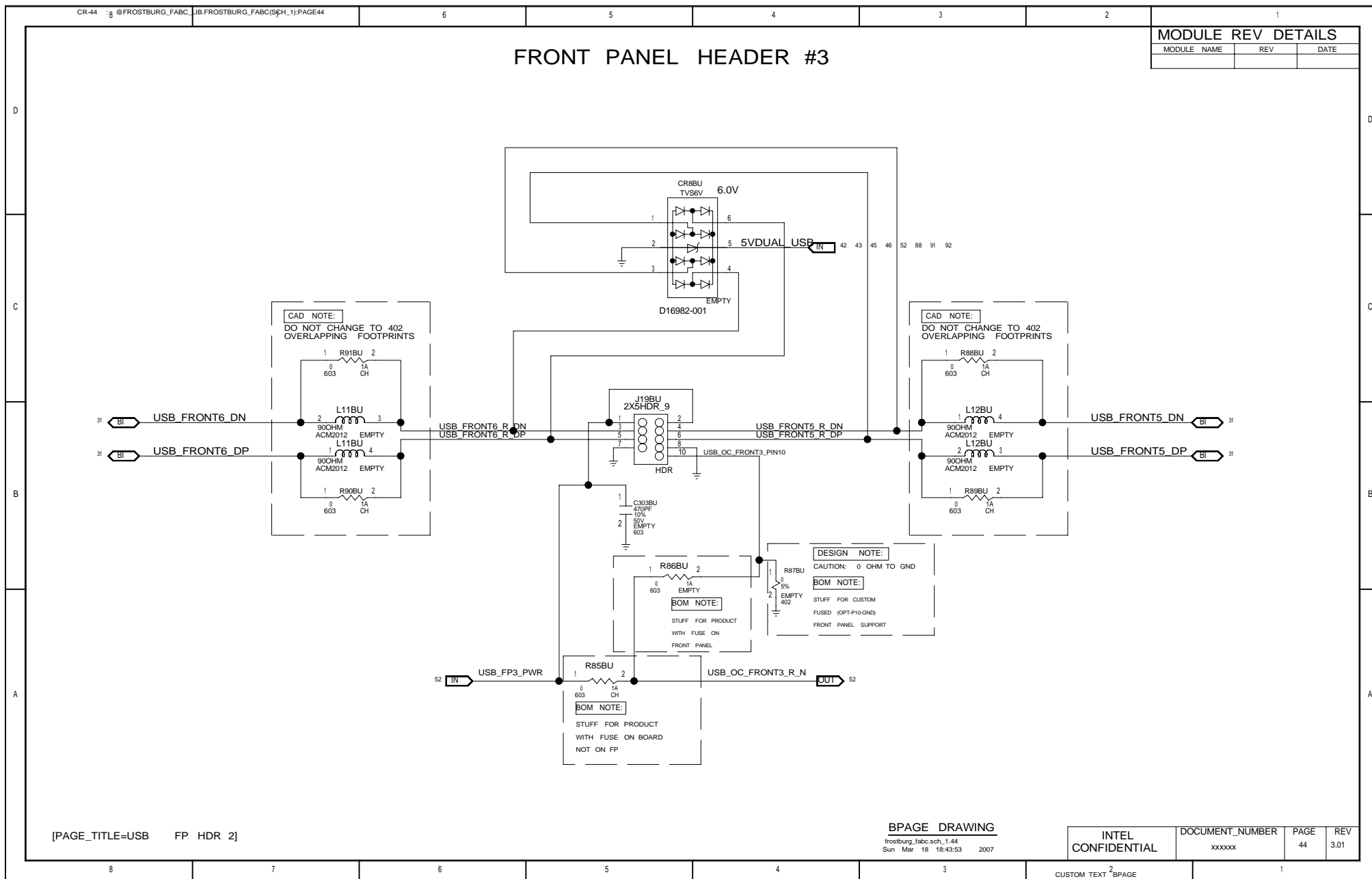


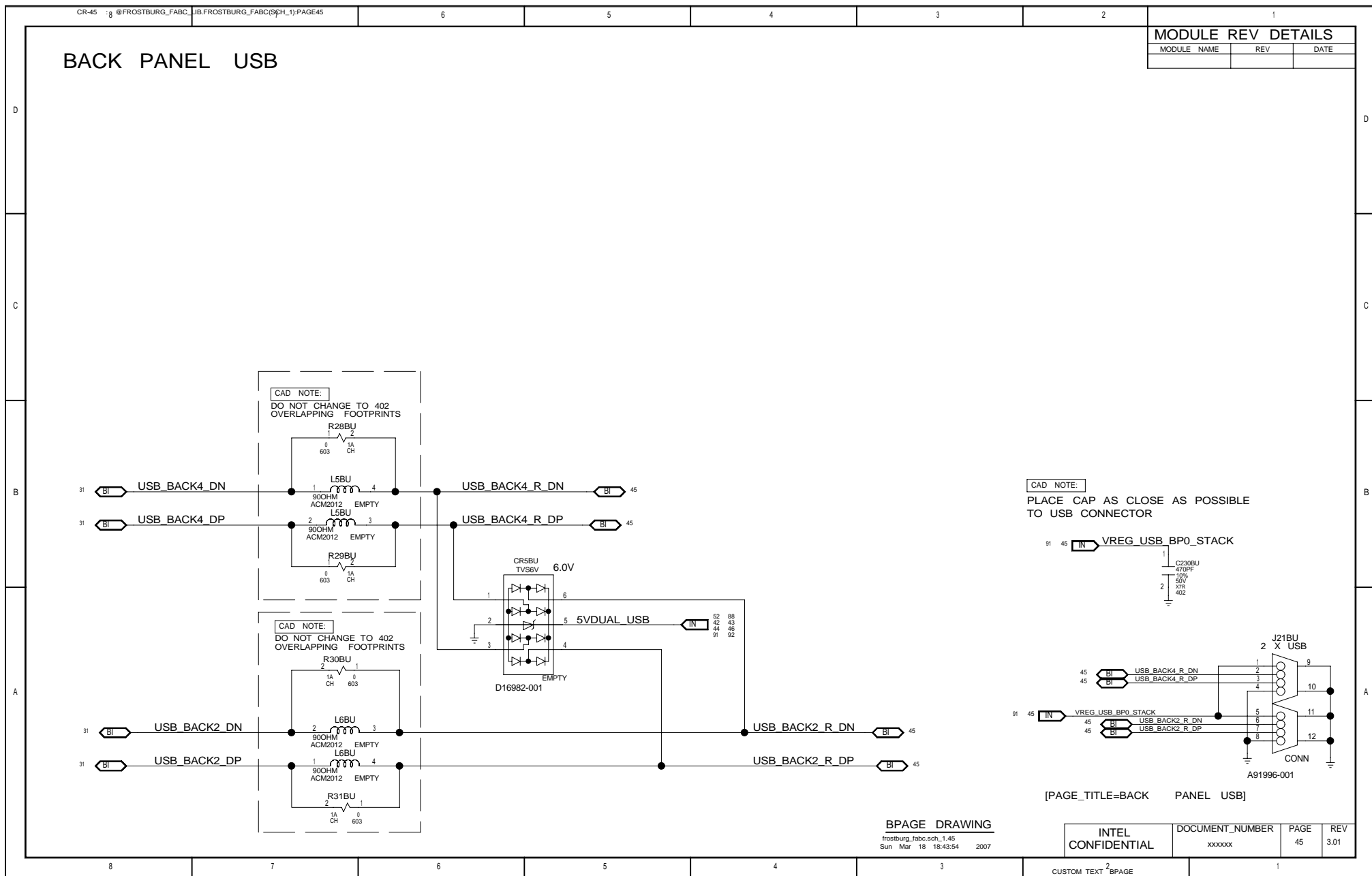


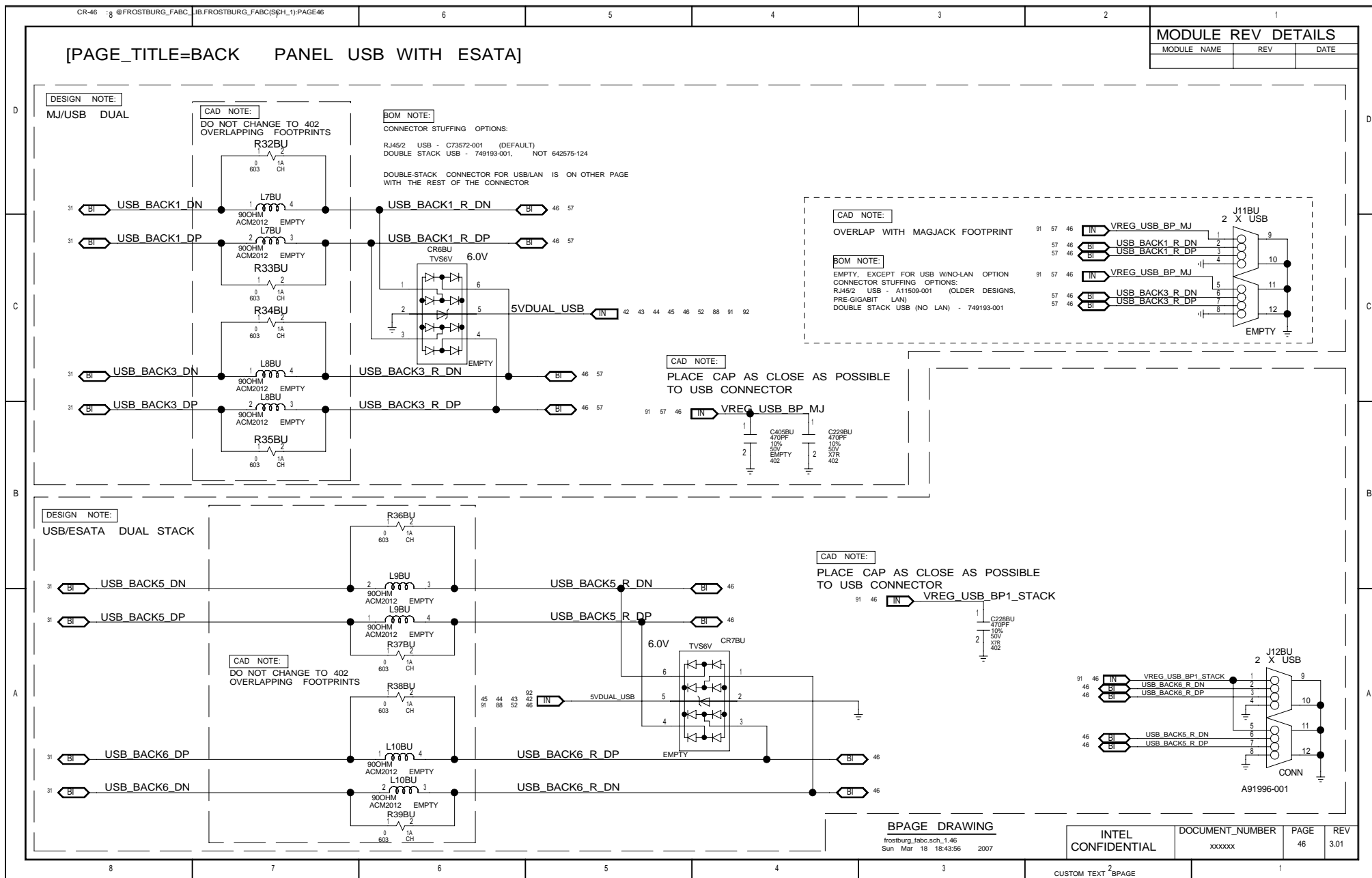


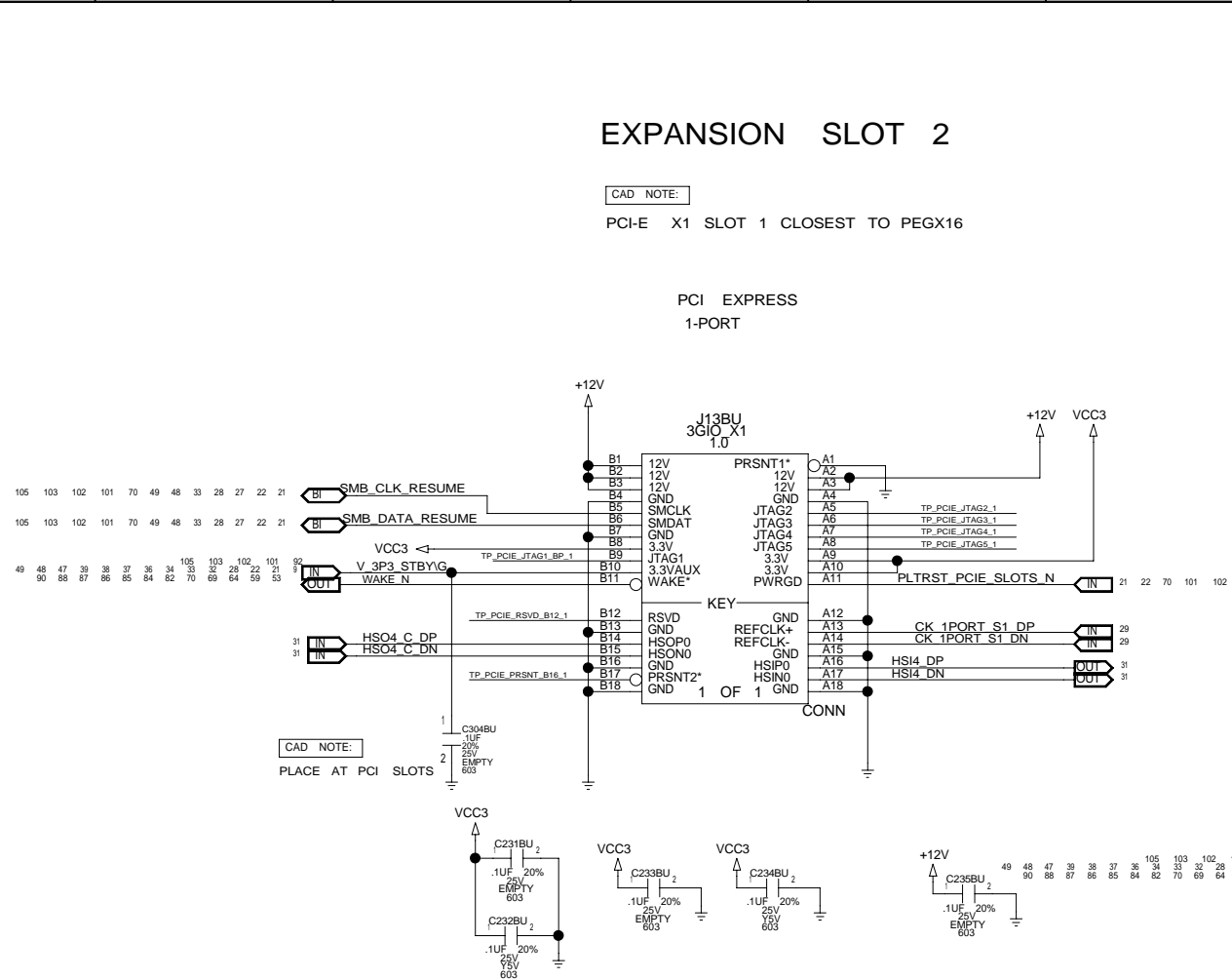












MODULE REV DETAILS		
MODULE NAME	REV	DATE

[PAGE_TITLE=PCI EXPRESS X1 #1]

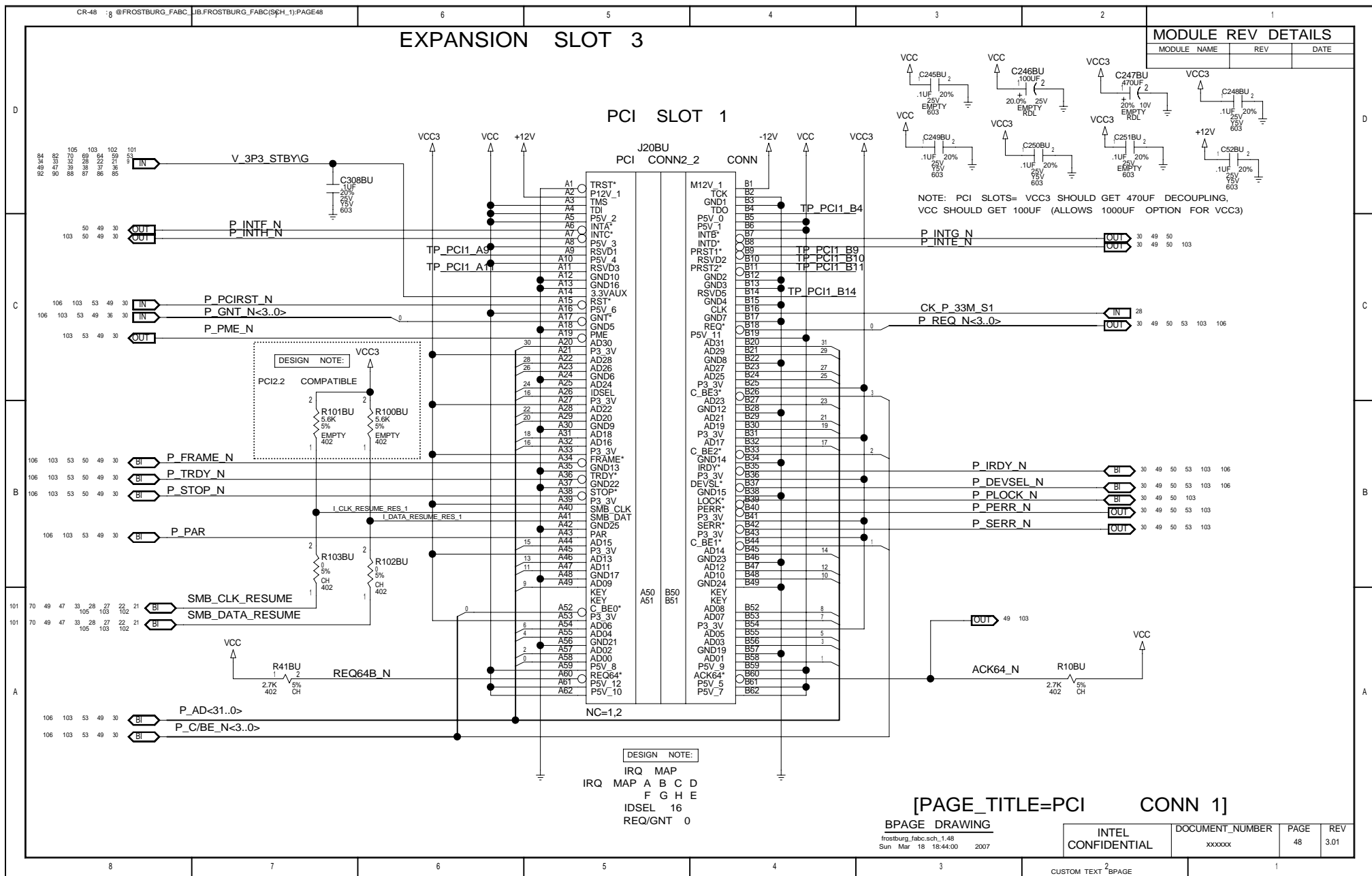
BPAGE DRAWING

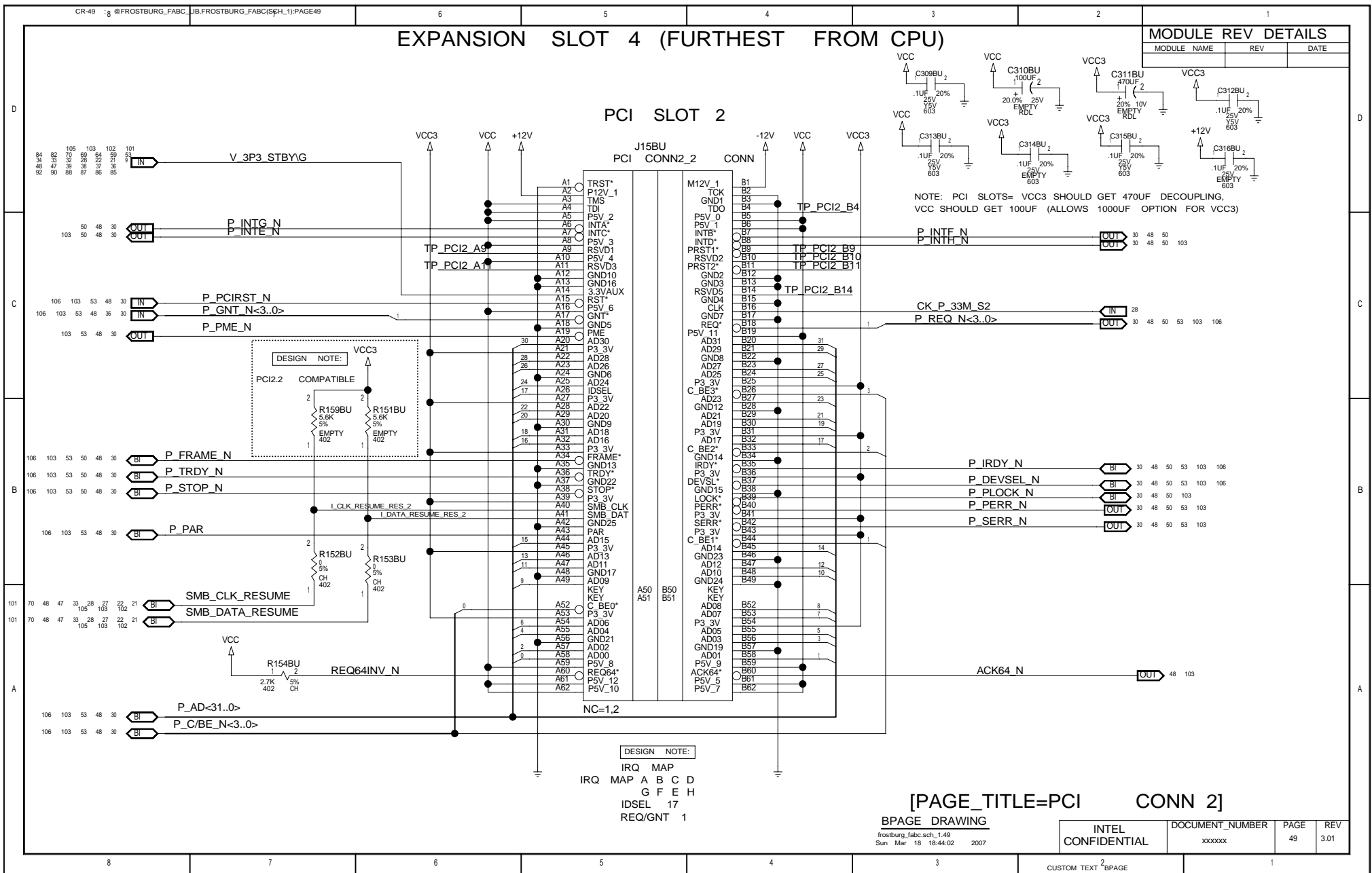
frostburg_fabc.sch_1.47
Sun Mar 18 18:43:58 2007

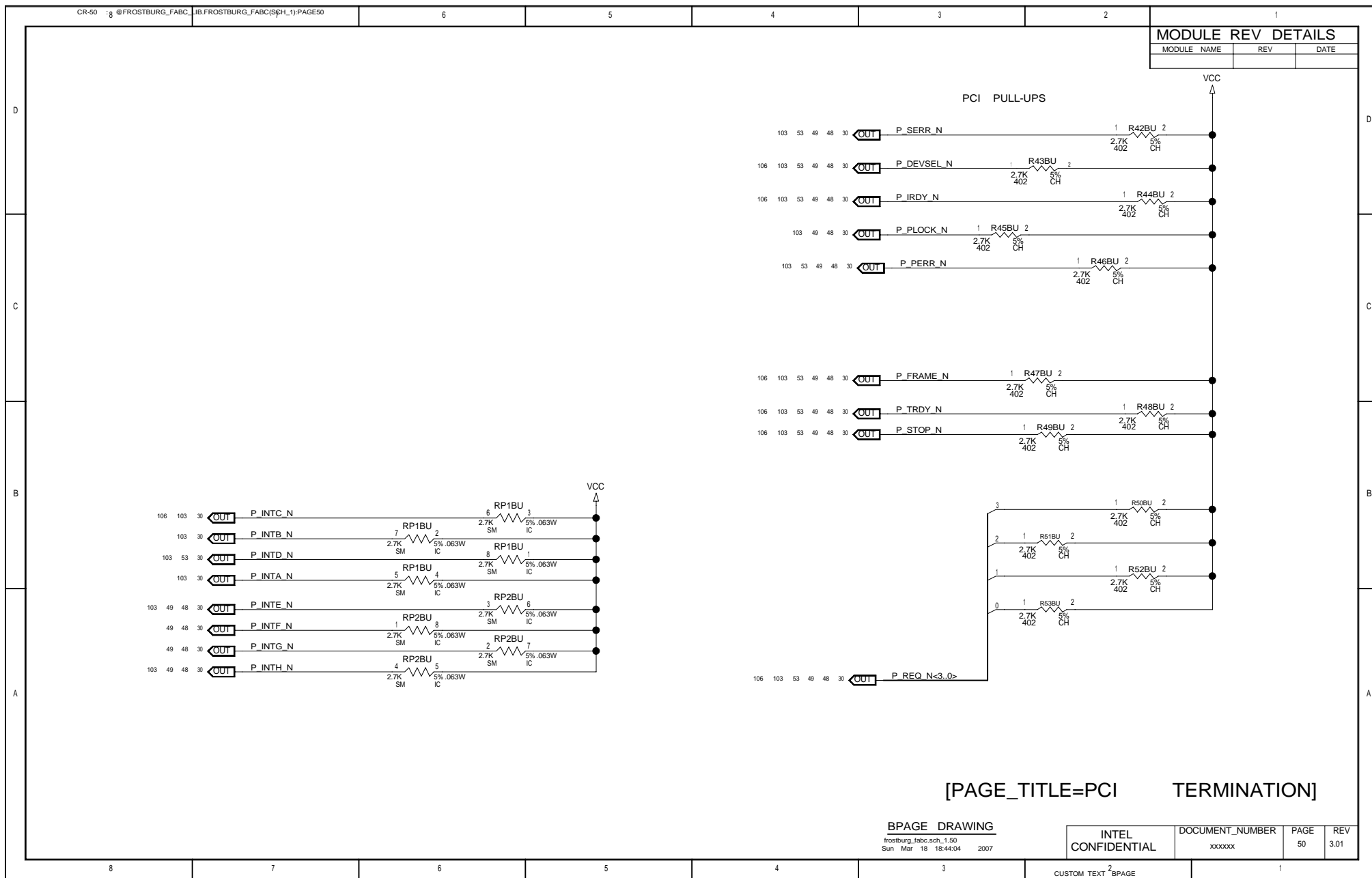
INTEL
CONFIDENTIAL

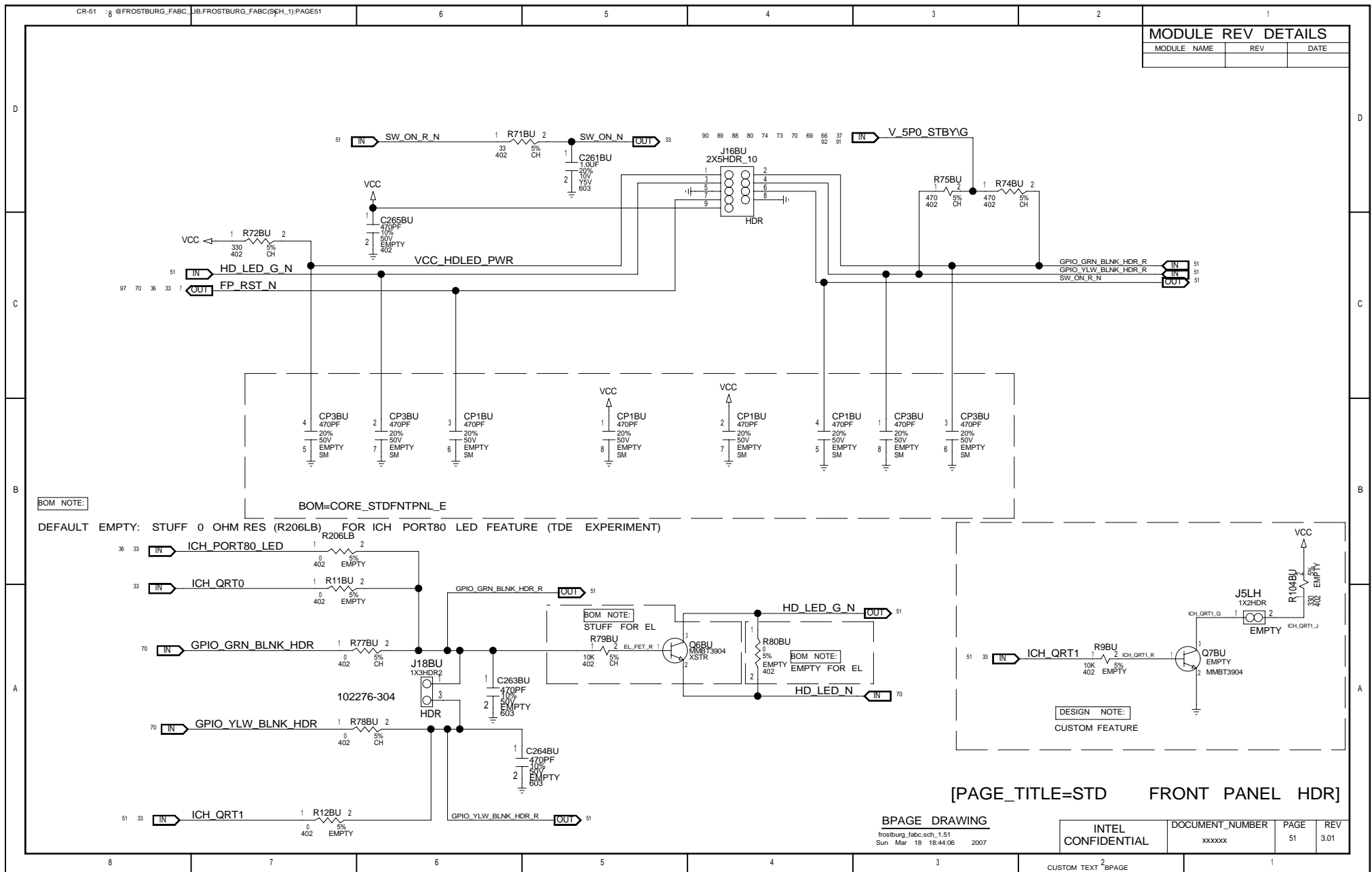
DOCUMENT_NUMBER
xxxxxxx

PAGE	REV
47	3.01





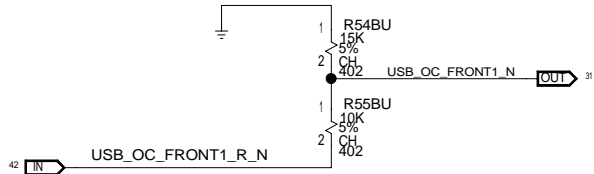




CR-52 : 8 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(S9H_1)-PAGE52

MODULE REV DETAILS		
MODULE NAME	REV	DATE

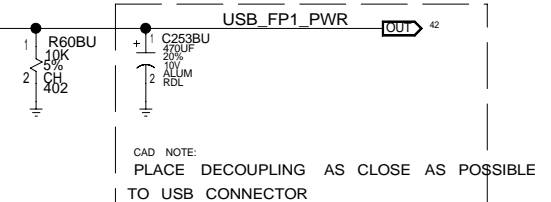
FRONT PANEL POWER #1



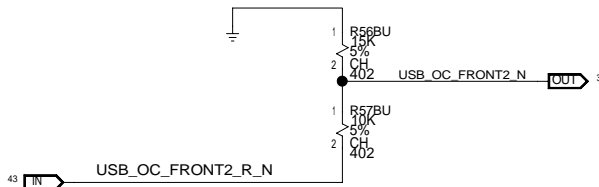
DESIGN NOTE:
STUFFING THE THERMISTOR ASSUMES FRONT PANEL CARD HAS NO FUSE AND DOES NOT PROVIDE OVER-CURRENT PROTECTION

CAD NOTE:
DUAL FOOTPRINT: PLACE 0 OHM 1206 IN PARALLEL WITH THERMISTOR

BOM NOTE:
STUFF 0 OHM INSTEAD OF THERMISTOR FOR PRODUCT WITH FUSE ON FRONT PANEL



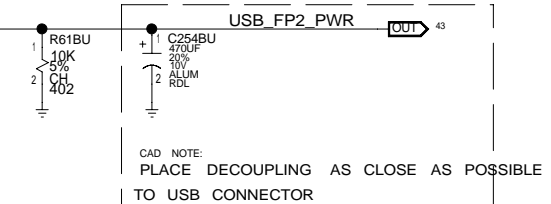
FRONT PANEL POWER #2



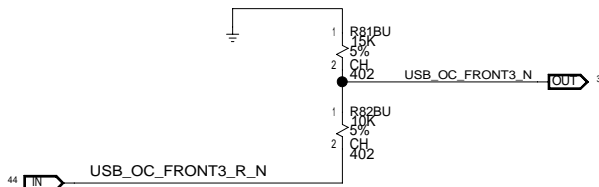
DESIGN NOTE:
STUFFING THE THERMISTOR ASSUMES FRONT PANEL CARD HAS NO FUSE AND DOES NOT PROVIDE OVER-CURRENT PROTECTION

CAD NOTE:
DUAL FOOTPRINT: PLACE 0 OHM 1206 IN PARALLEL WITH THERMISTOR

BOM NOTE:
STUFF 0 OHM INSTEAD OF THERMISTOR FOR PRODUCT WITH FUSE ON FRONT PANEL



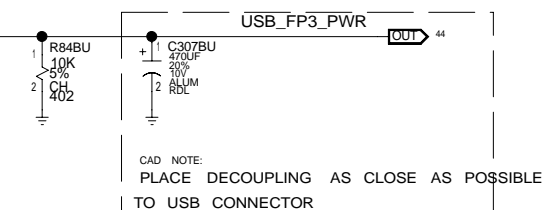
FRONT PANEL POWER #3



DESIGN NOTE:
STUFFING THE THERMISTOR ASSUMES FRONT PANEL CARD HAS NO FUSE AND DOES NOT PROVIDE OVER-CURRENT PROTECTION

CAD NOTE:
DUAL FOOTPRINT: PLACE 0 OHM 1206 IN PARALLEL WITH THERMISTOR

BOM NOTE:
STUFF 0 OHM INSTEAD OF THERMISTOR FOR PRODUCT WITH FUSE ON FRONT PANEL



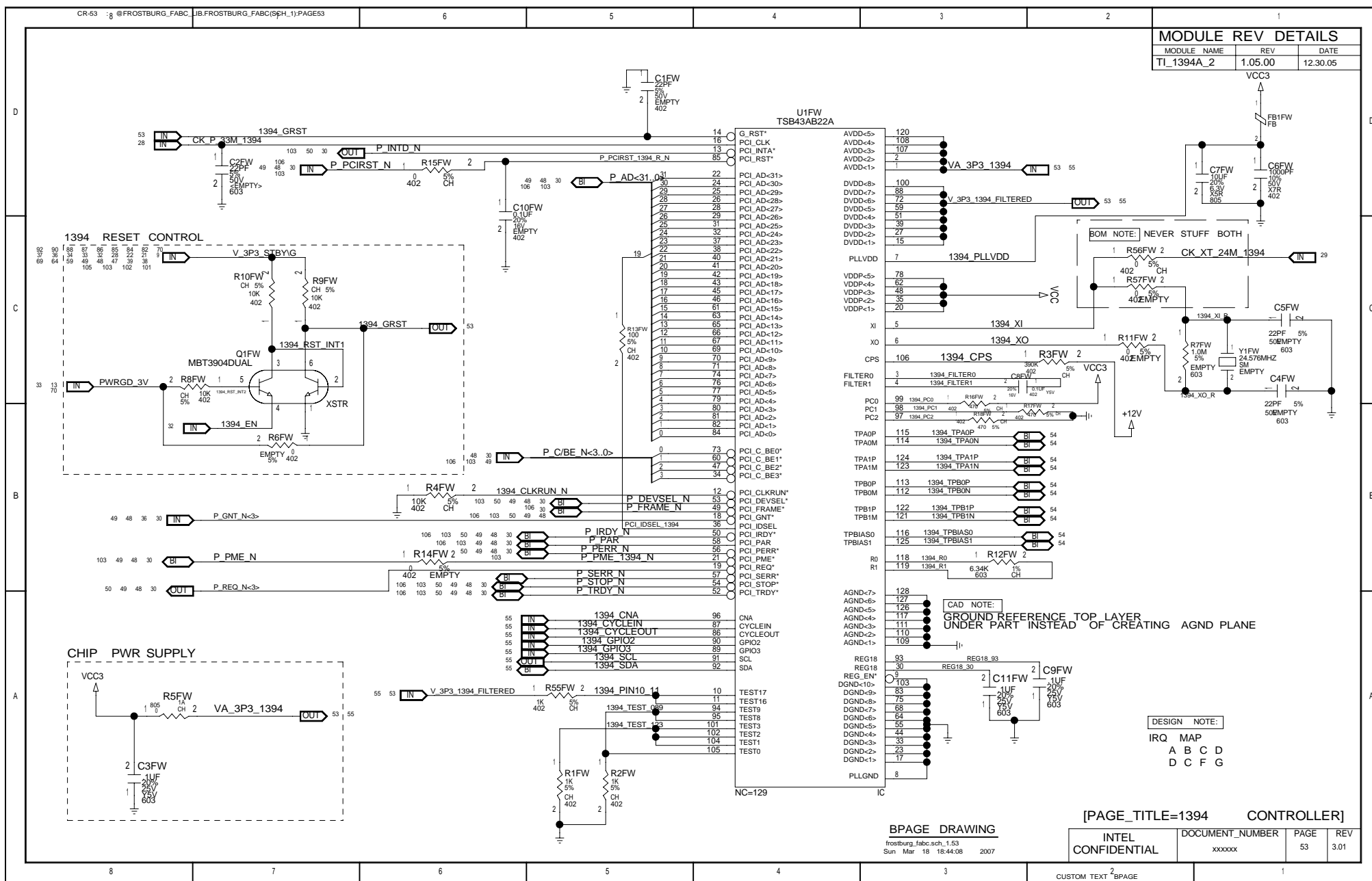
BPAGE DRAWING

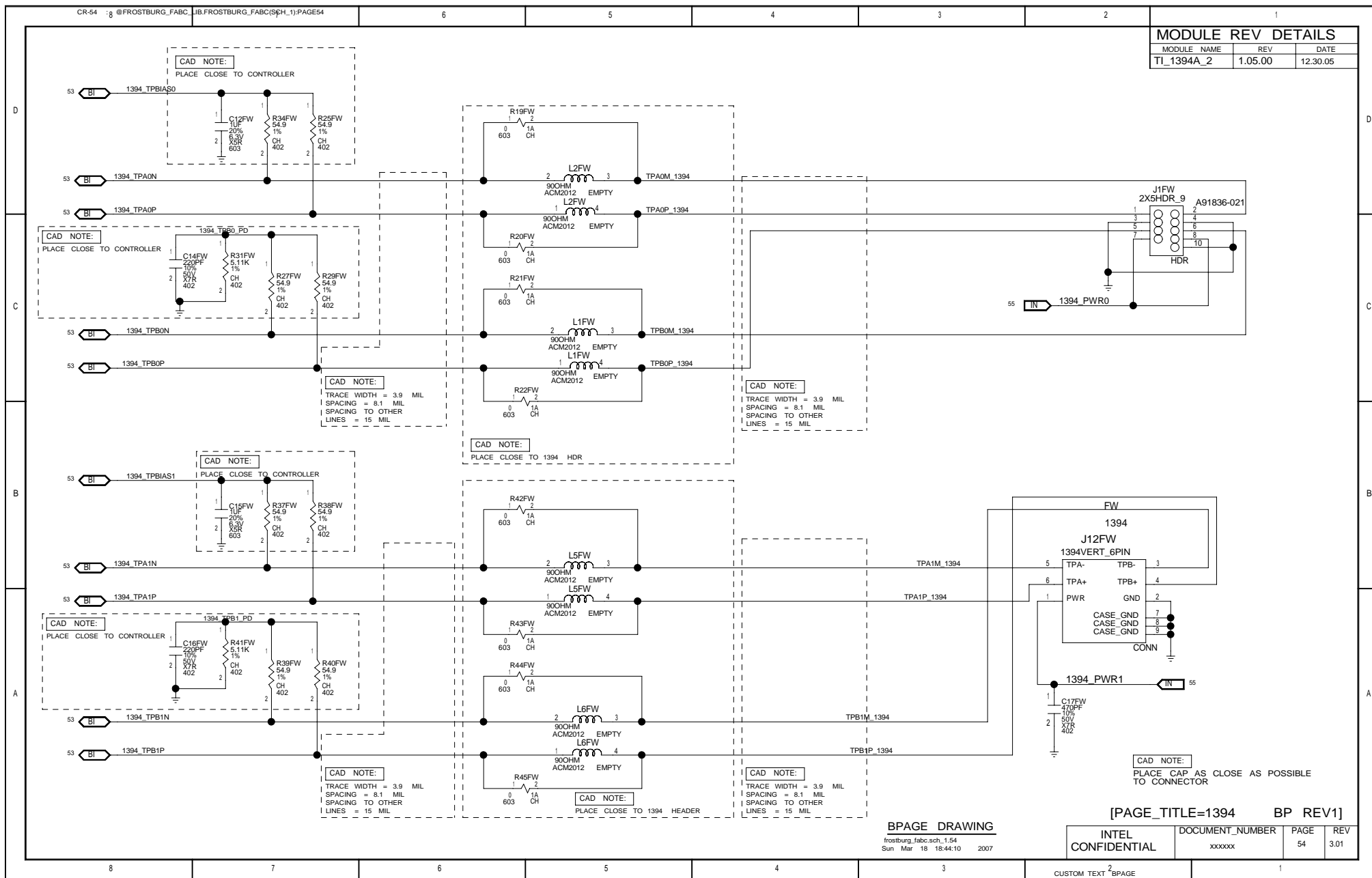
frostburg_fabc.sch, 1.52
Sun Mar 18 18:44:07 2007

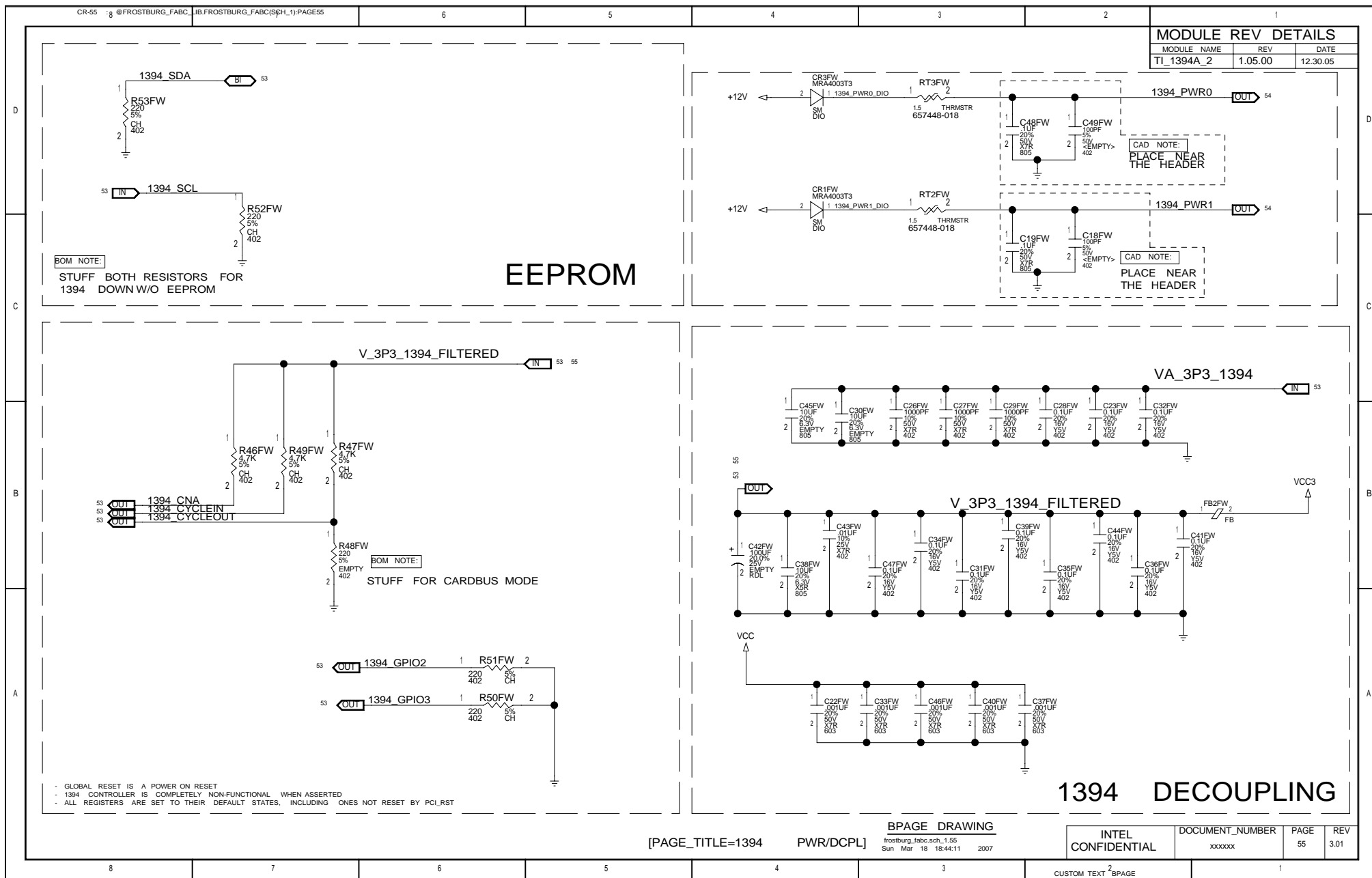
[PAGE_TITLE=USB_FP_HEADER_POWER]

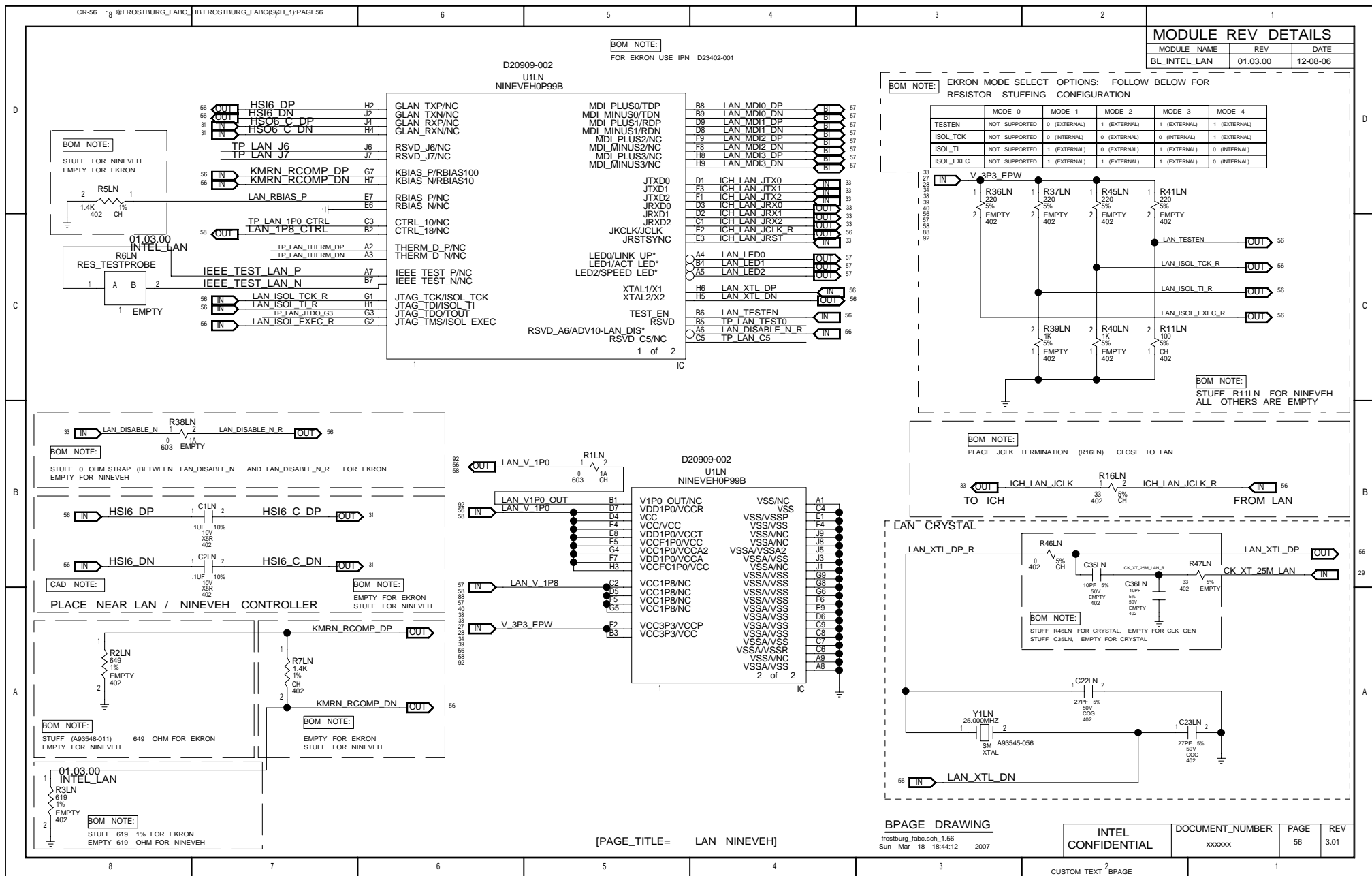
INTEL CONFIDENTIAL	DOCUMENT NUMBER xxxxxx	PAGE 52	REV 3.01
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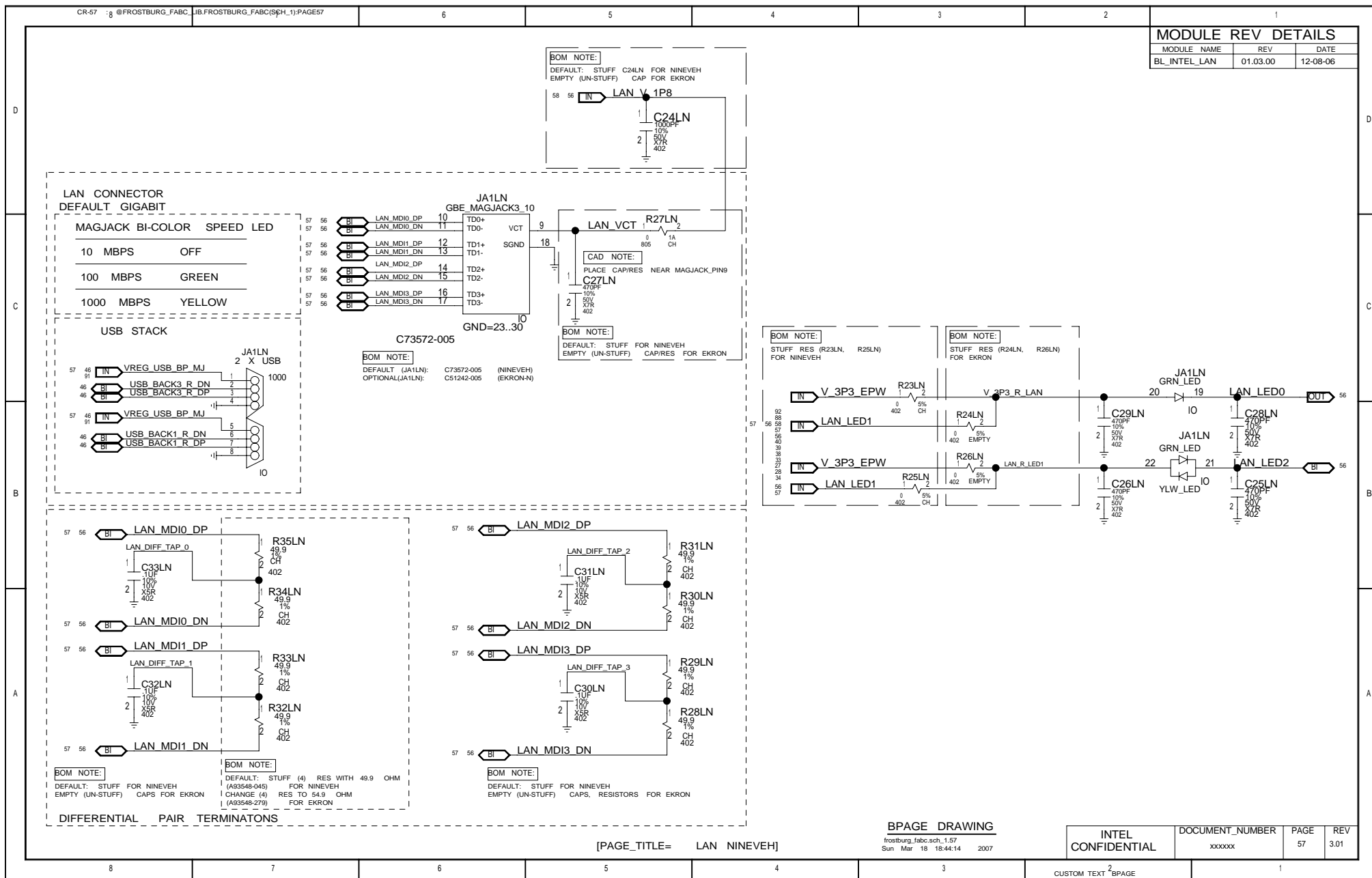
CUSTOM TEXT 2 BPAGE





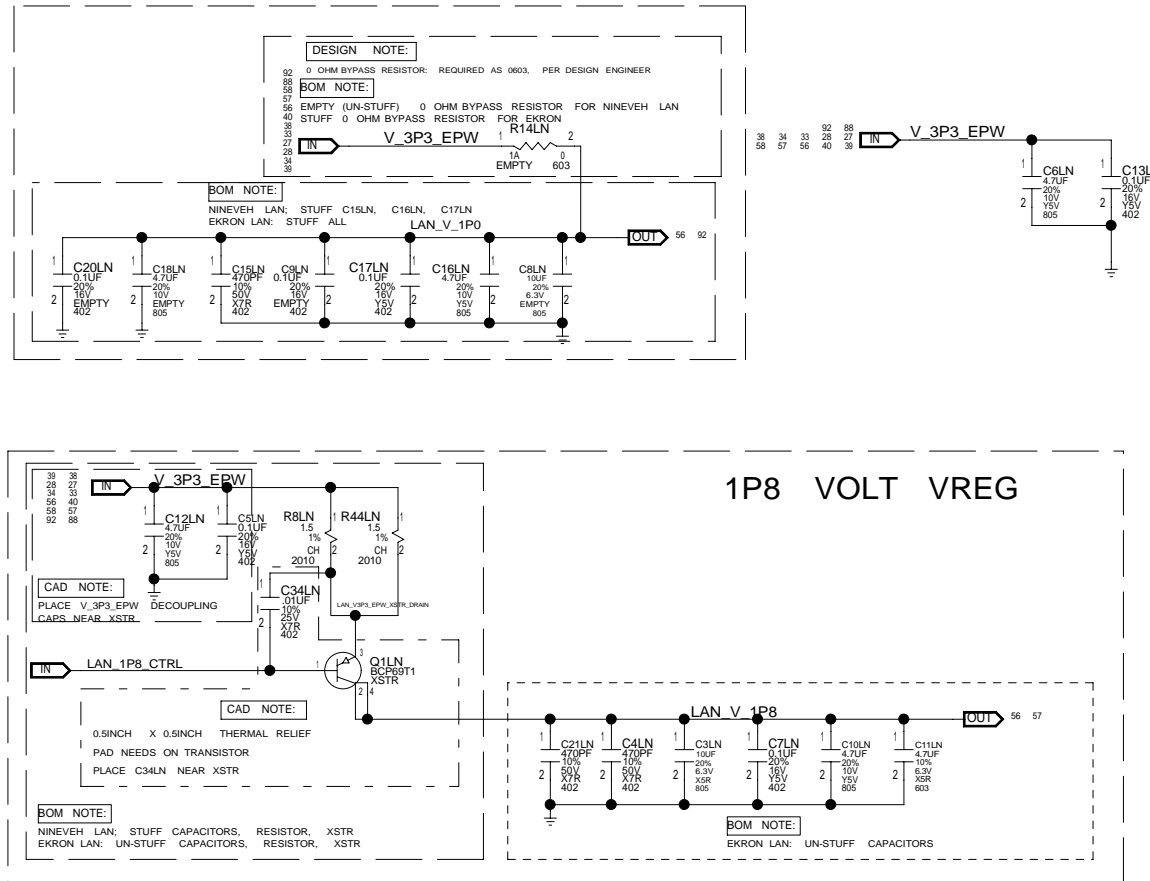






CR-58 : 8 @FROSTBURG_FABC LIB.FROSTBURG_FABC(S9H_1)-PAGE58

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_INTEL_LAN	01.03.00	12-08-06



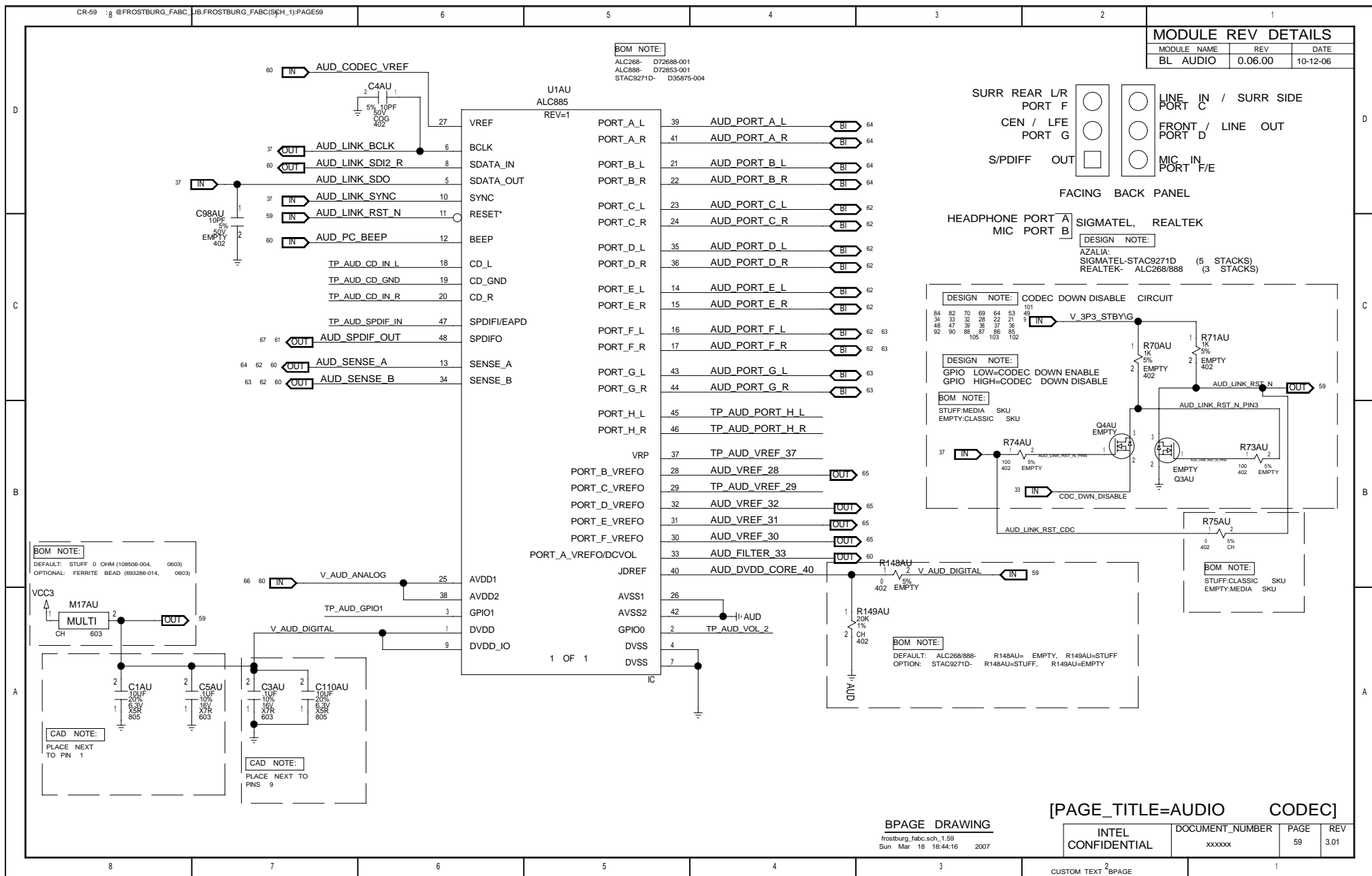
[PAGE_TITLE= LAN NINEVEH]

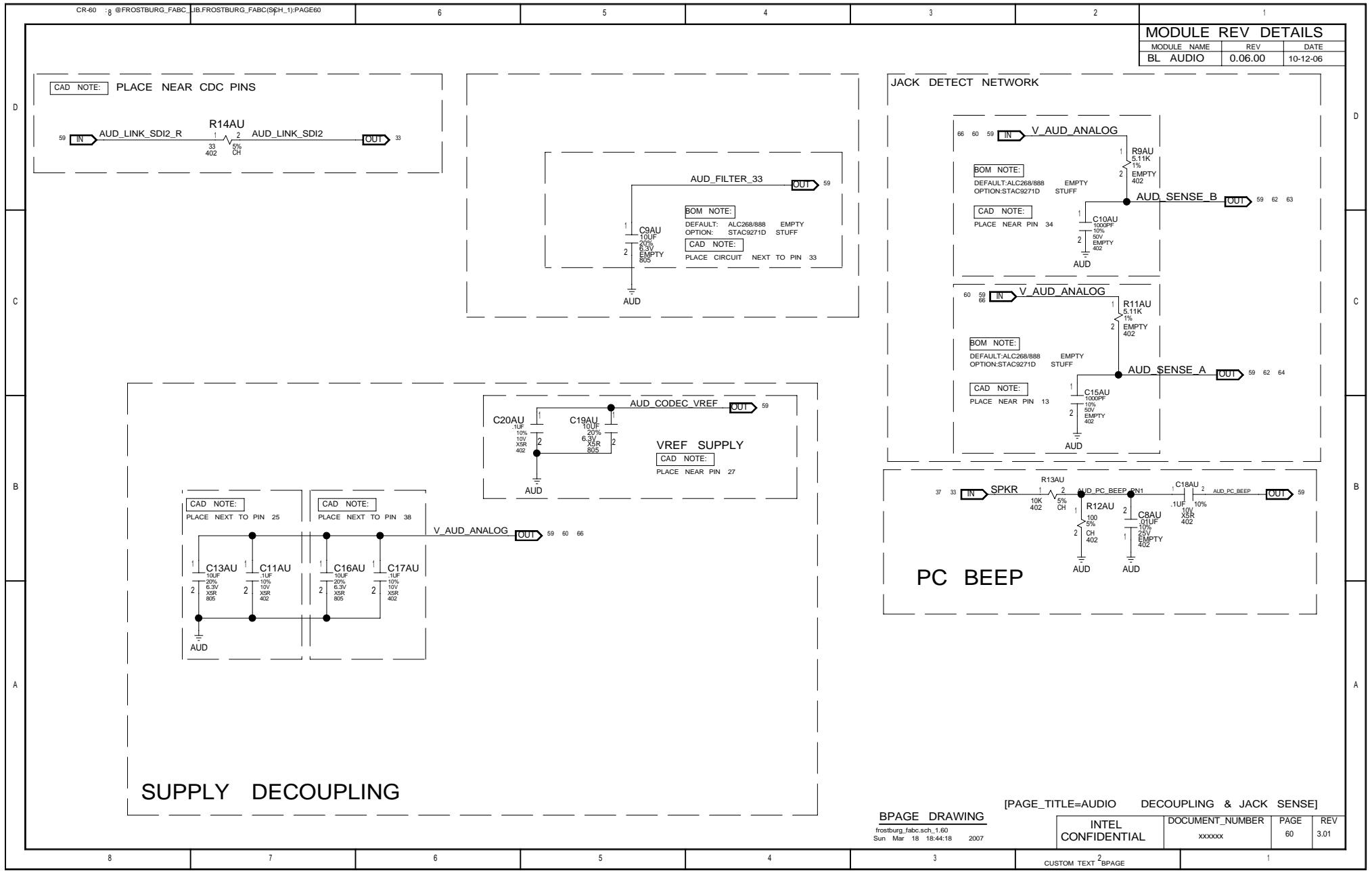
BPAGE DRAWING

frostburg_fabc.sch.1.58
Sun Mar 18 18:44:15 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxxx	58	3.01

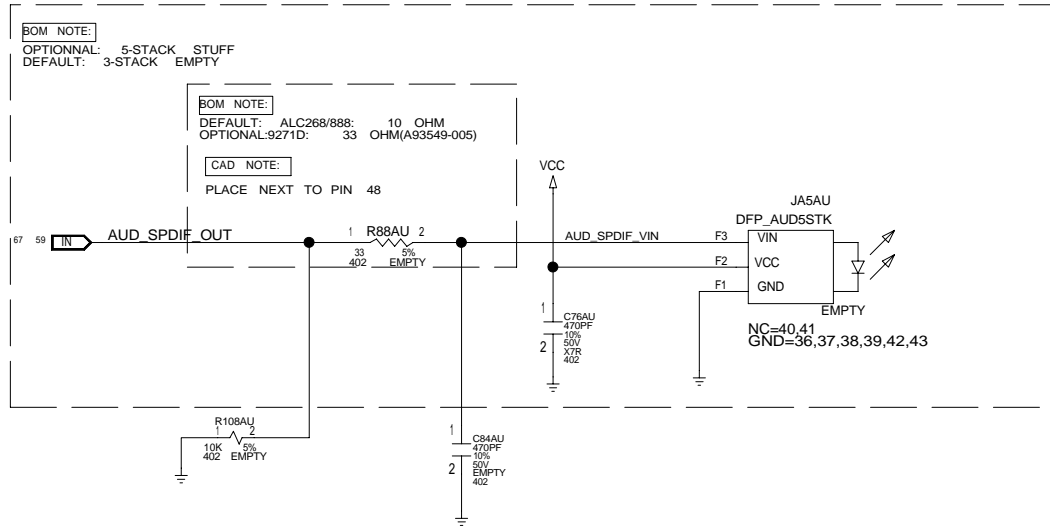
CUSTOM TEXT 2 BPAGE





CR-61 : 8 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(S&H_1)-PAGE61

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL AUDIO	0.06.00	10-12-06



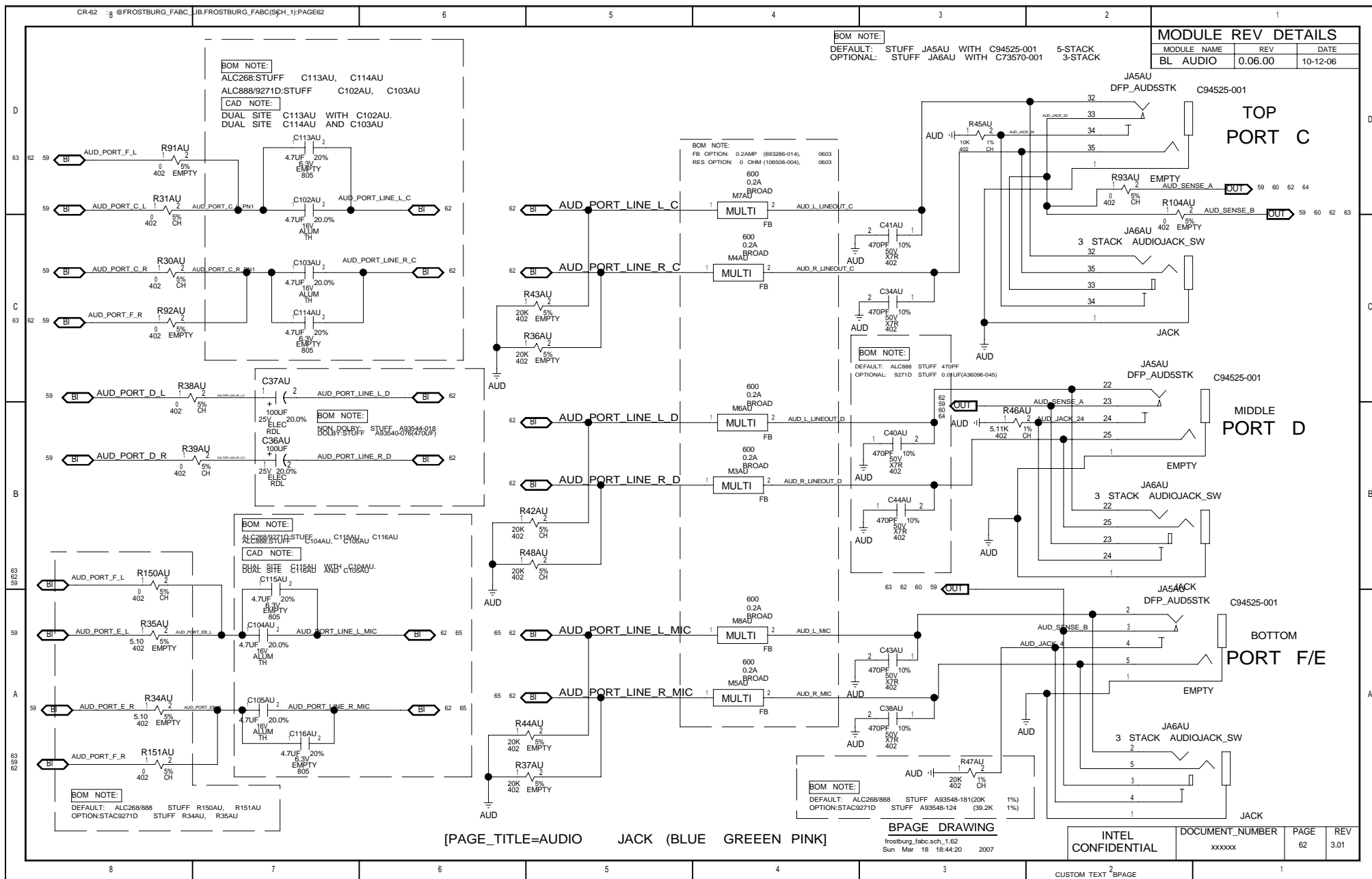
[PAGE_TITLE=AUDIO SPDIF]

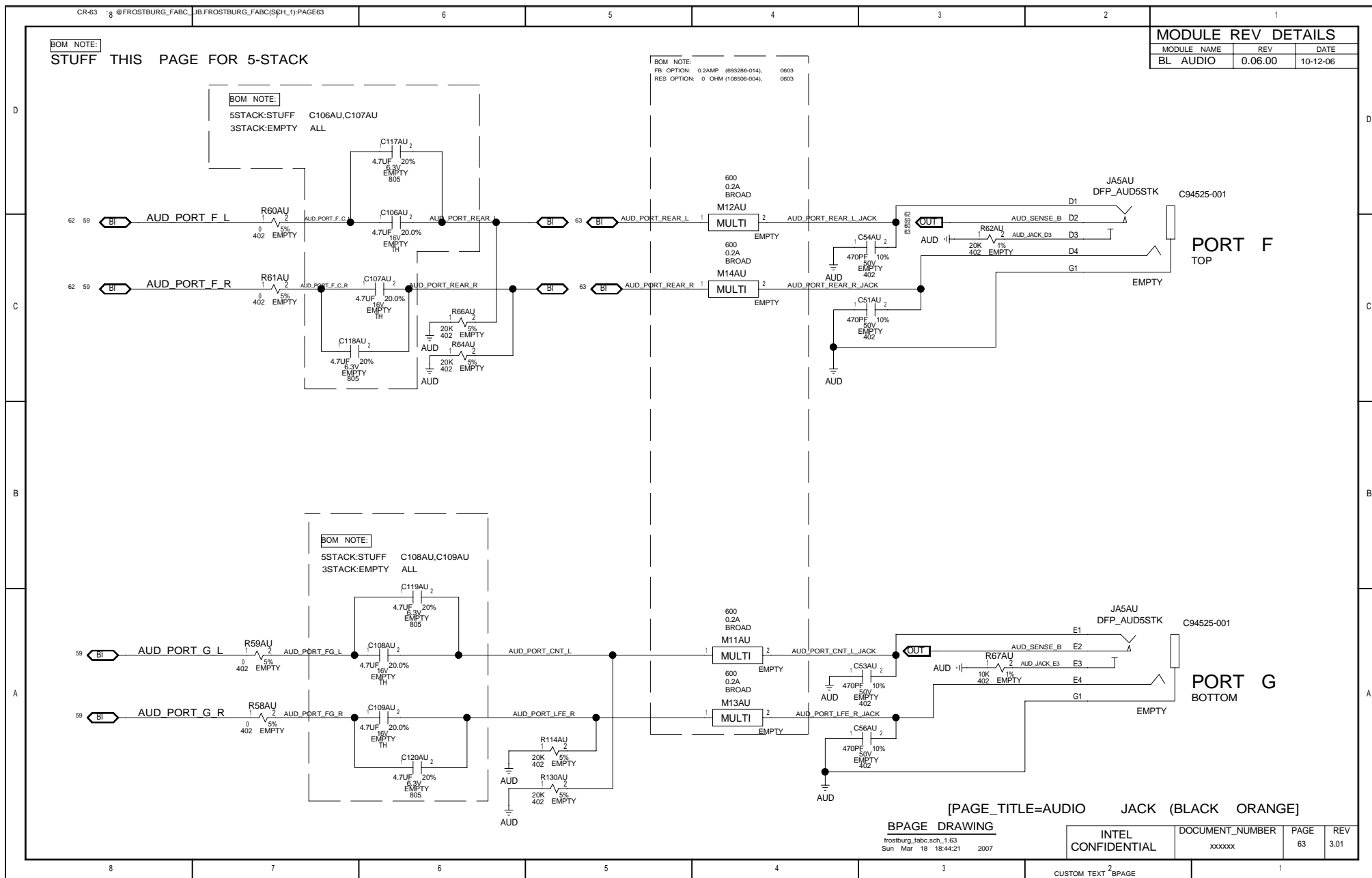
BPAGE DRAWING

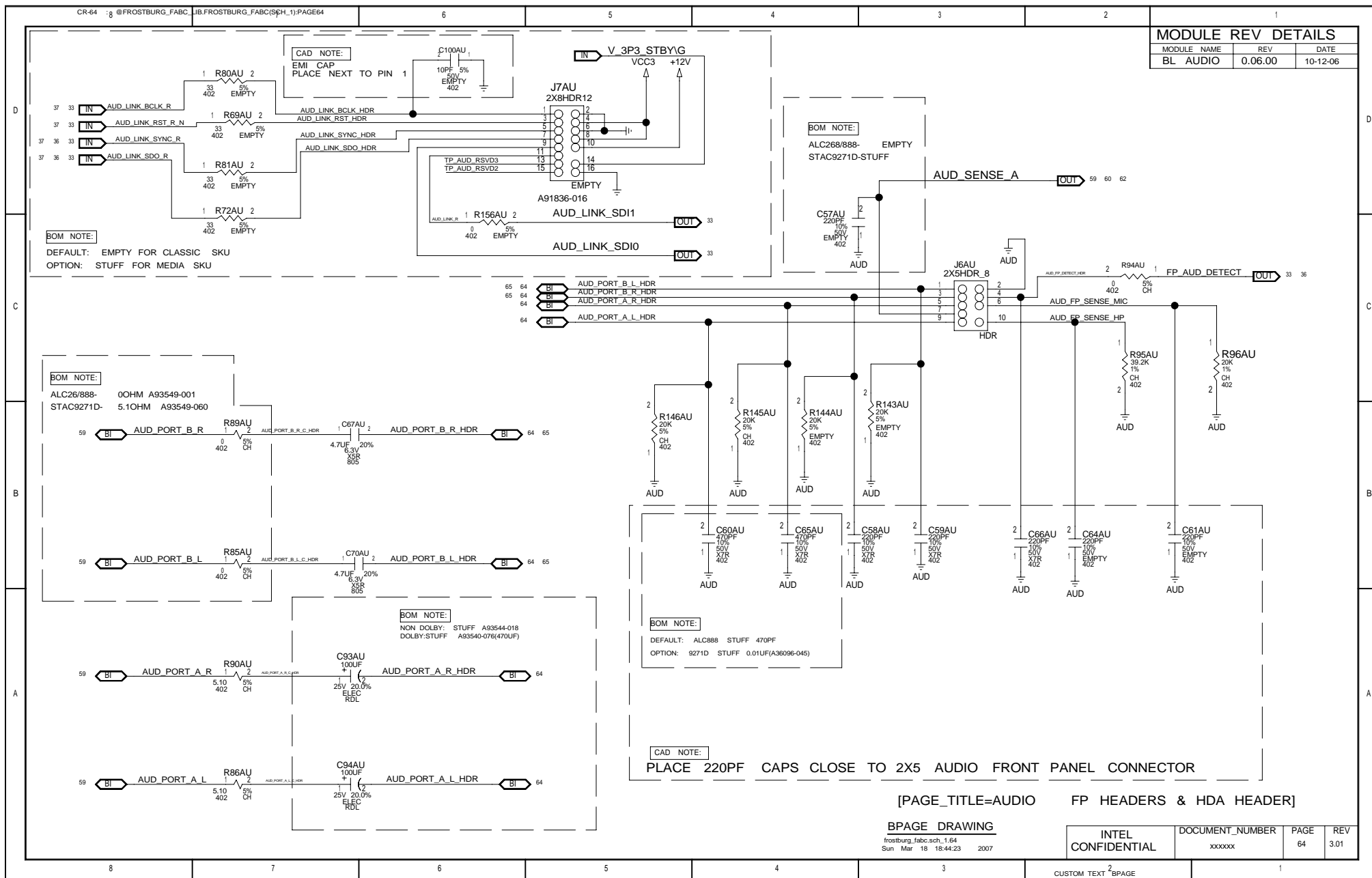
frostburg_fabc.sch, 1.61
Sun Mar 18 18:44:19 2007

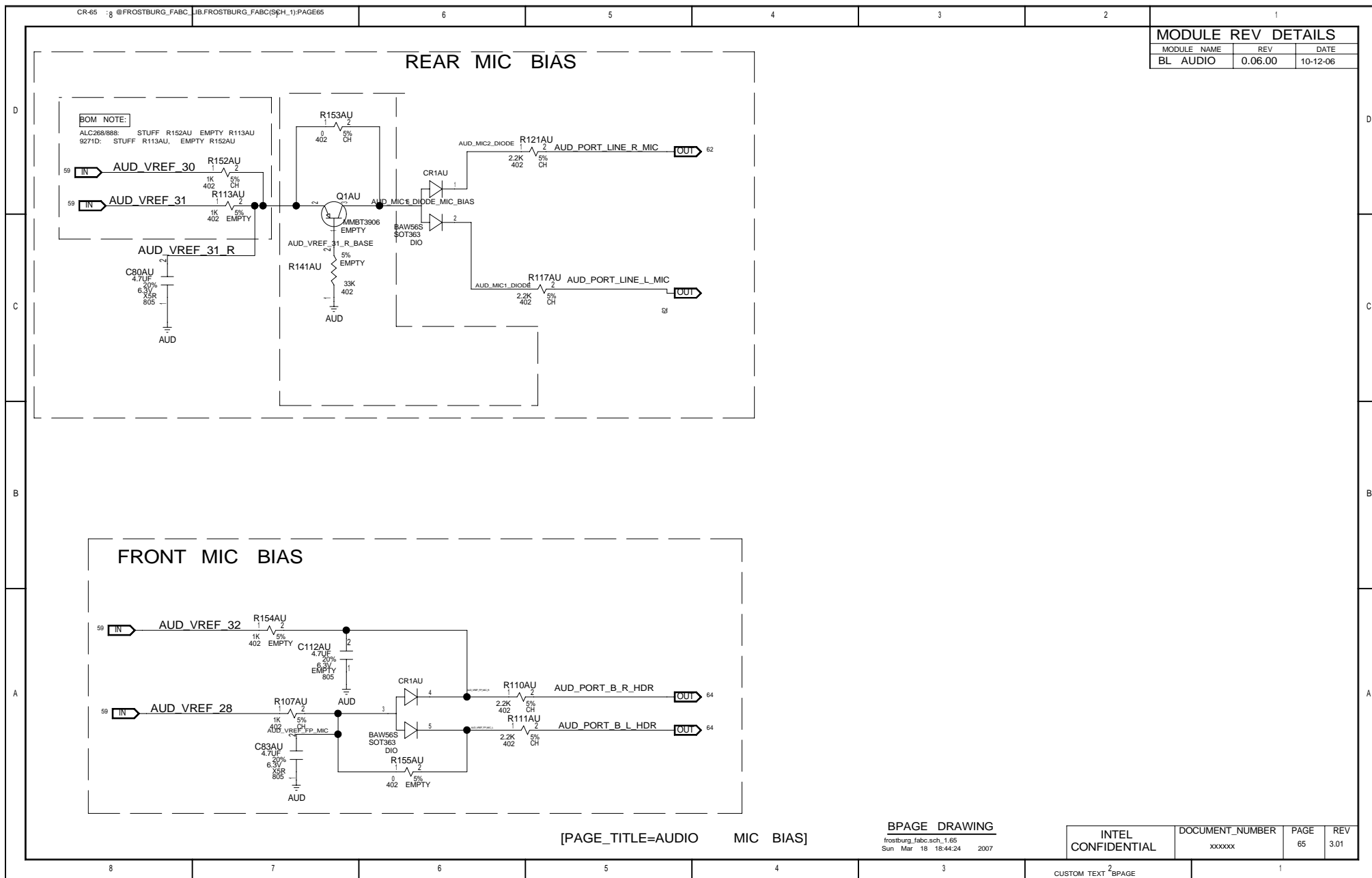
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 61	REV 3.01
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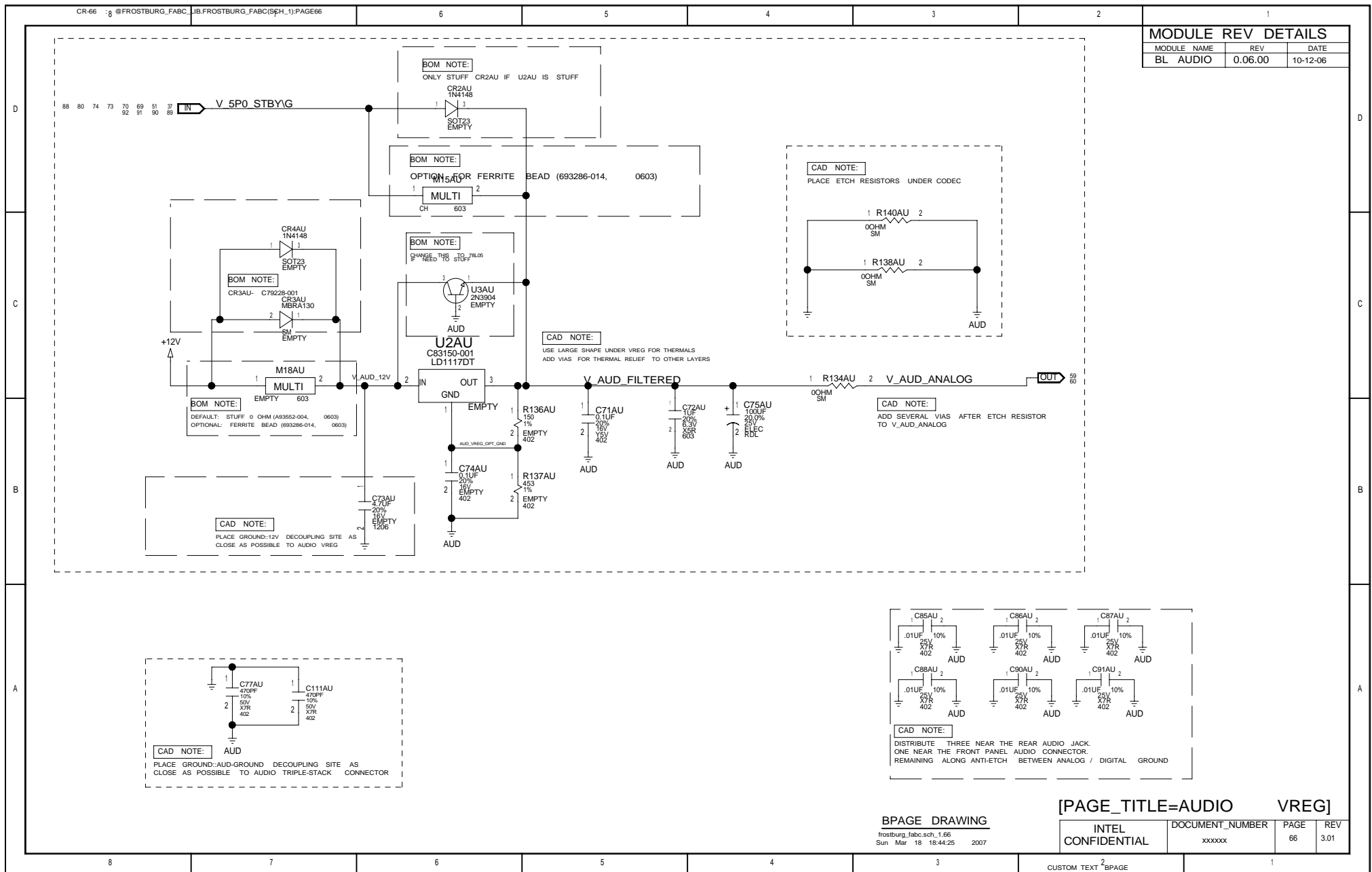
CUSTOM TEXT 2 BPAGE







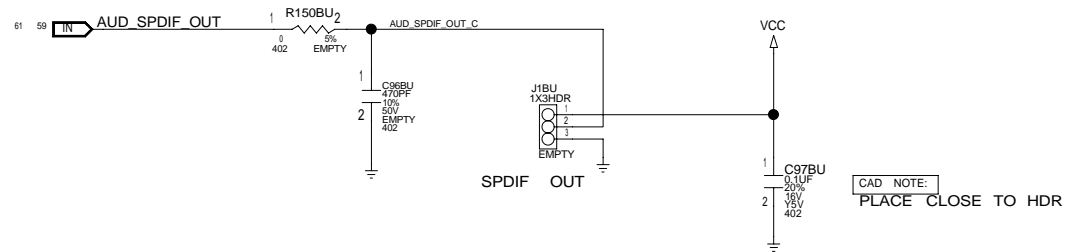




CR-67 : 8 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(S&H_1):PAGE67

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL AUDIO	0.06.00	10-12-06

ATX CUSTOM SPDIF HEADER



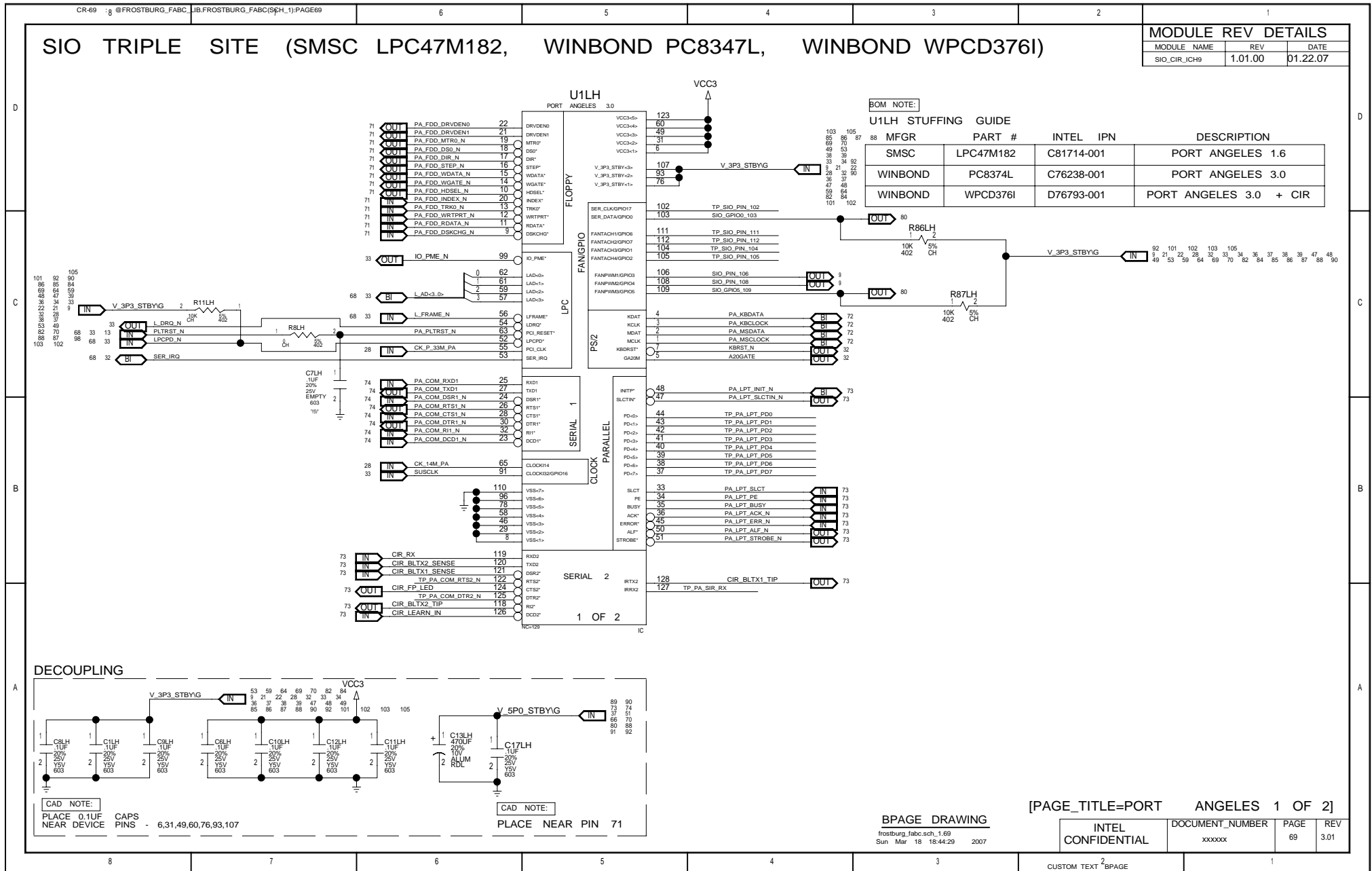
BPAGE DRAWING

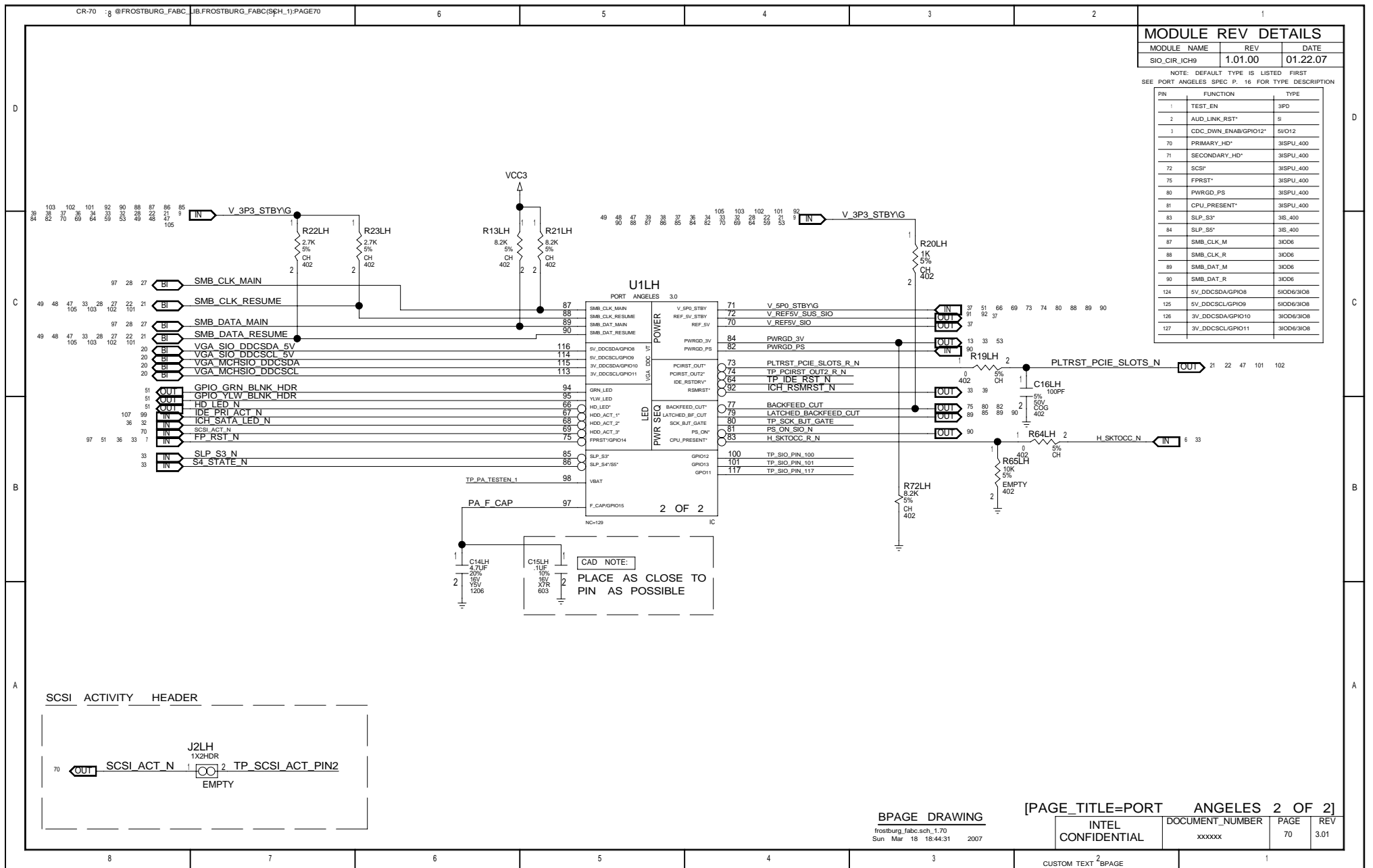
frostburg_fabc.sch, 1.67
Sun Mar 18 18:44:27 2007

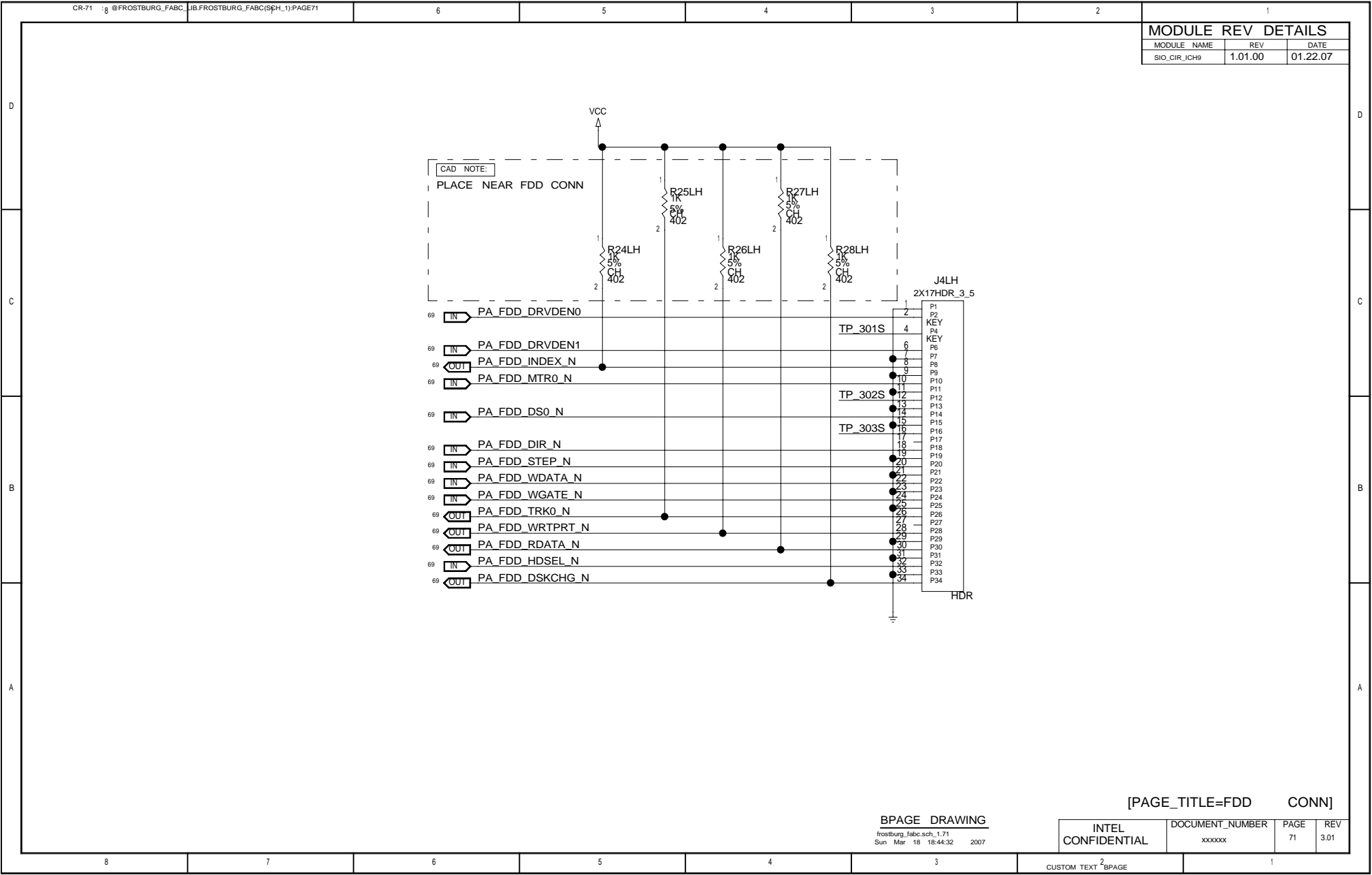
[PAGE_TITLE=SPDIF HEADER]

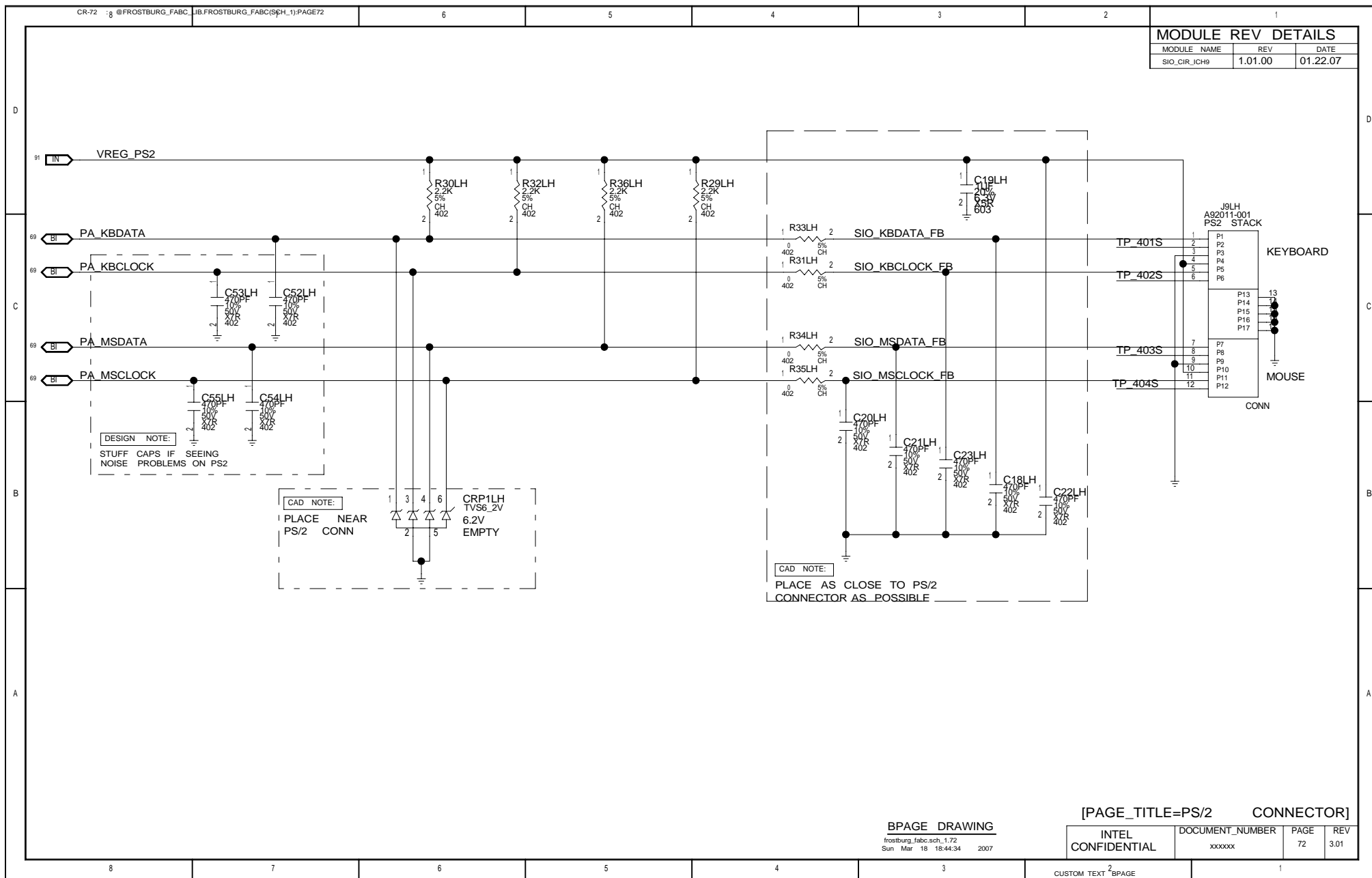
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxxx	PAGE 67	REV 3.01
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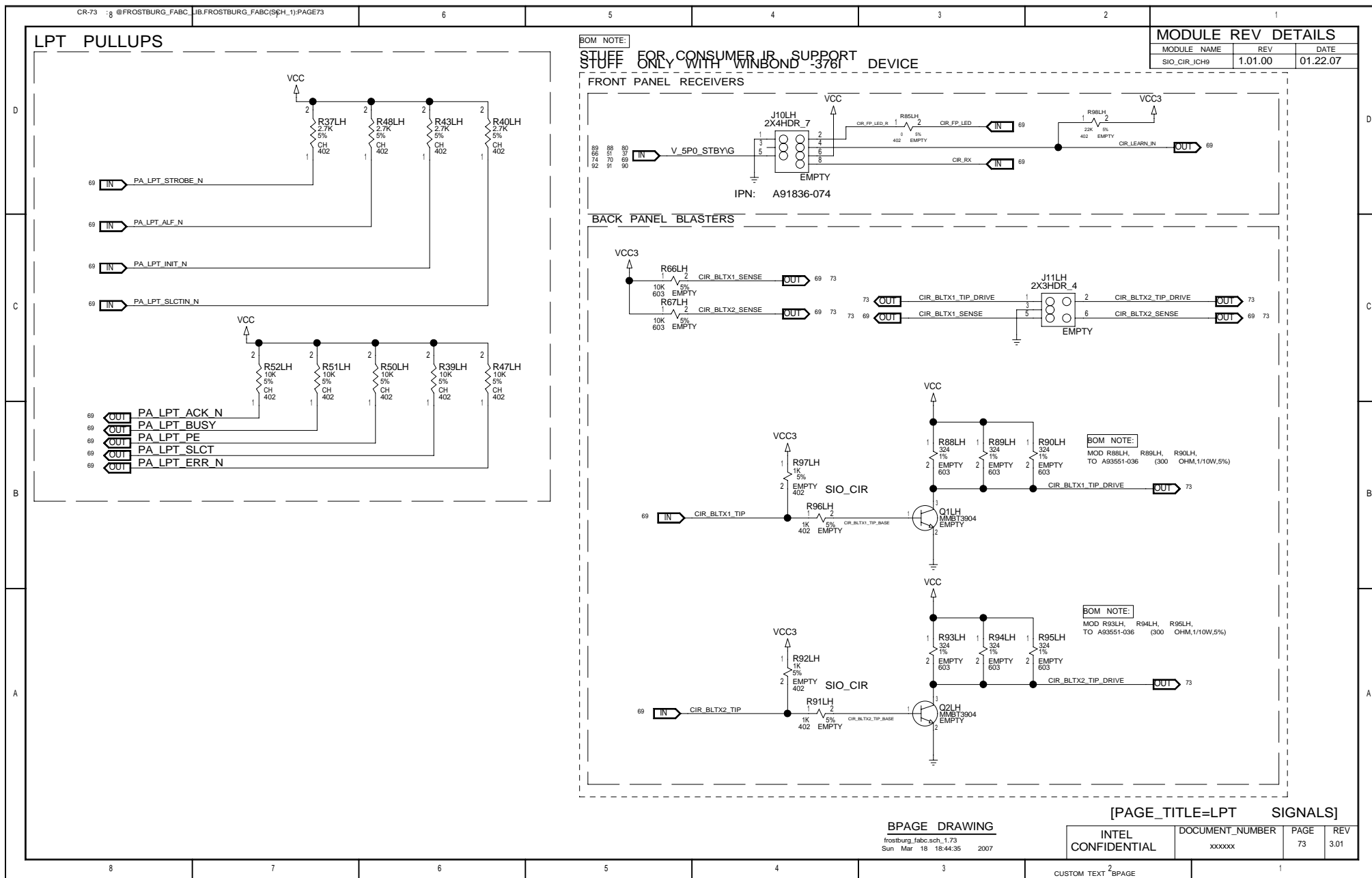
CUSTOM TEXT 2_BPAGE

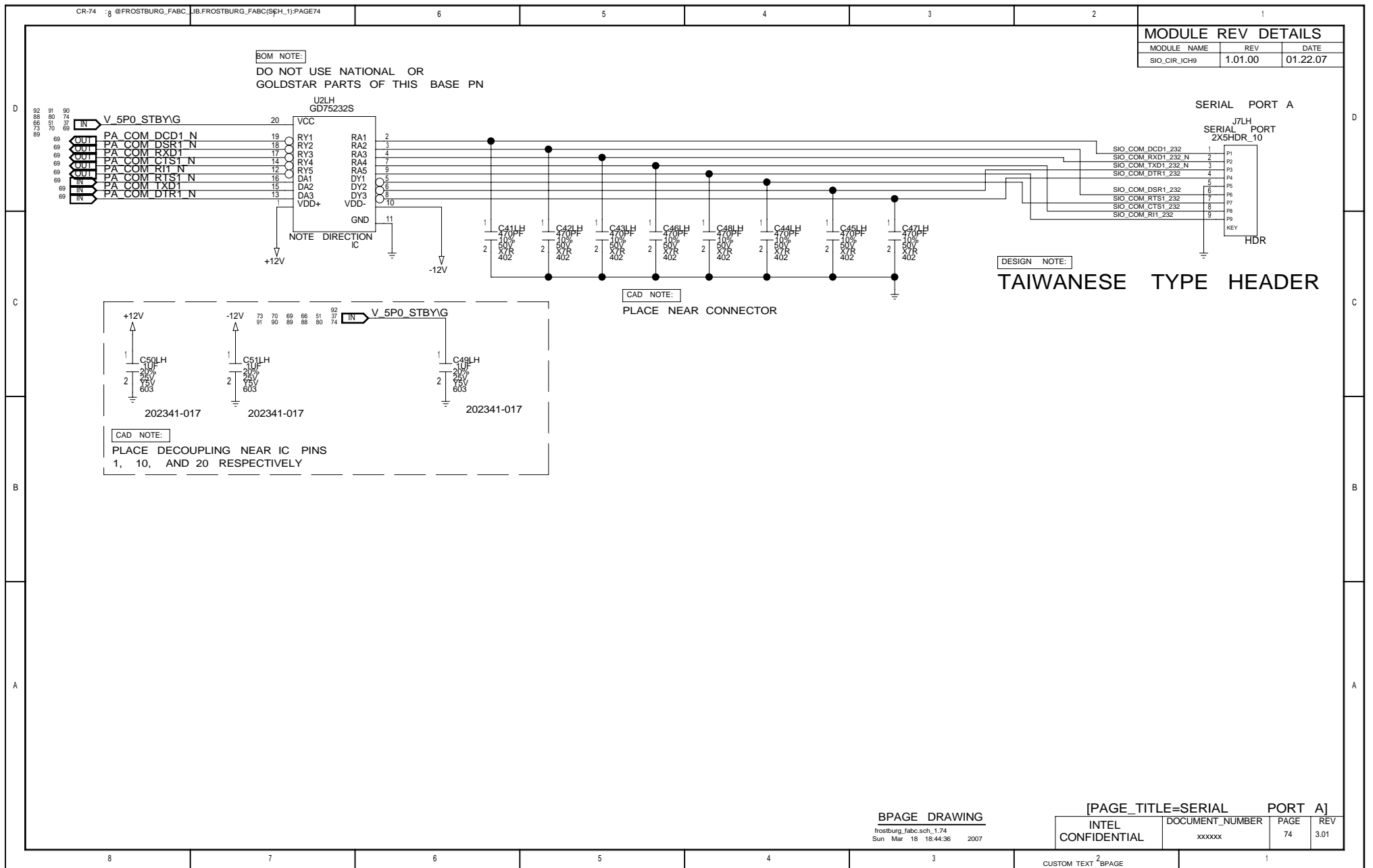












CR-75 : 8 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(S9H_1)-PAGE75

65342312

MODULE REV DETAILS		
MODULE NAME	REV	DATE
SUPER_IO	1.08.01	2.10.06

D

C

B

A

PASSIVE BLEED CIRCUIT

BPAGE DRAWING

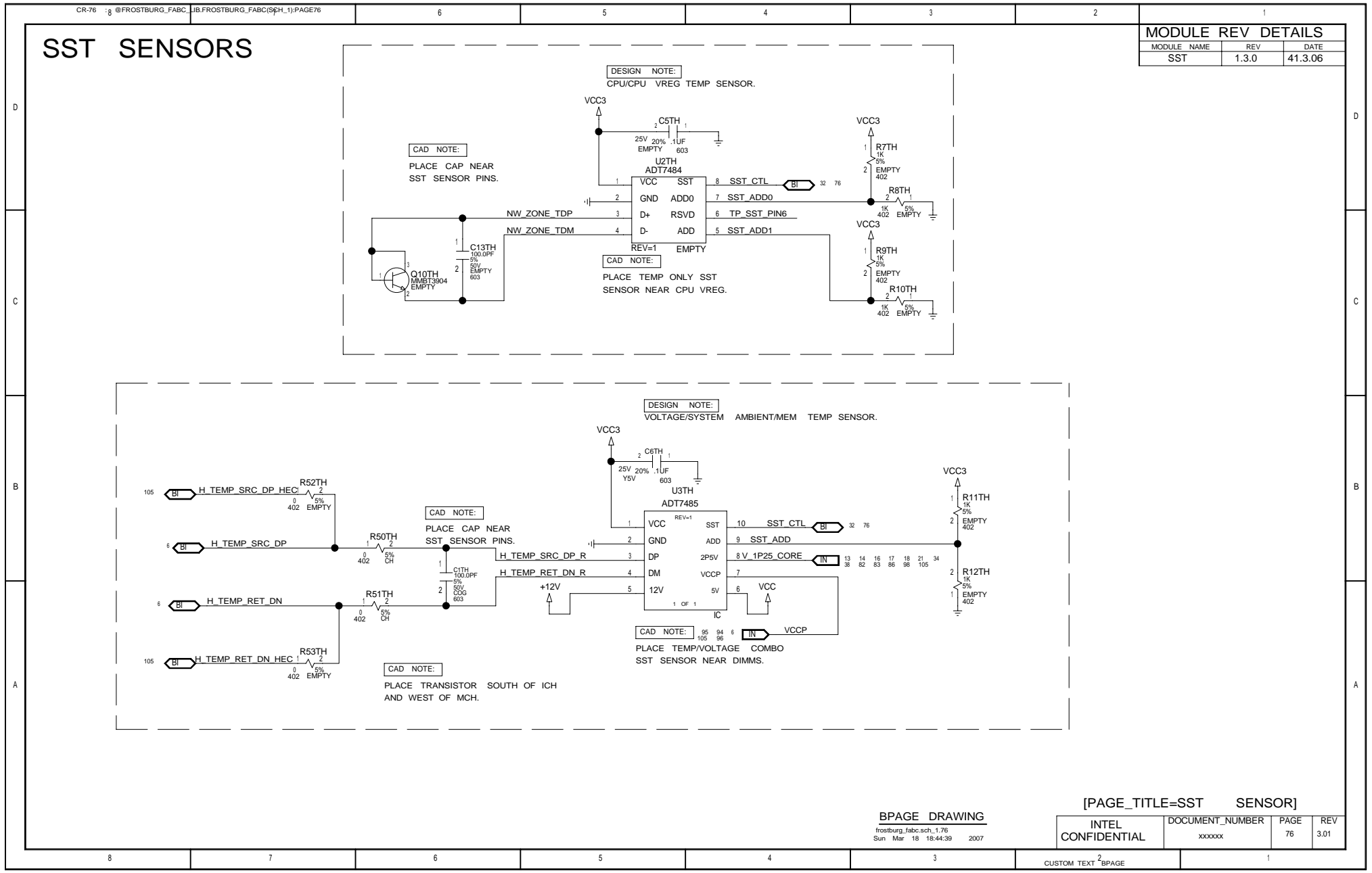
frostburg_fabc.sch, 1.75
Sun Mar 18 18:44:38 2007

[PAGE_TITLE=STUDIES PURPOSE]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 75	REV 3.01
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CUSTOM TEXT 2BPAGE

1



BPAGE DRAWING

frostburg_fabc.sch_1.76
Sun Mar 18 18:44:39 2007

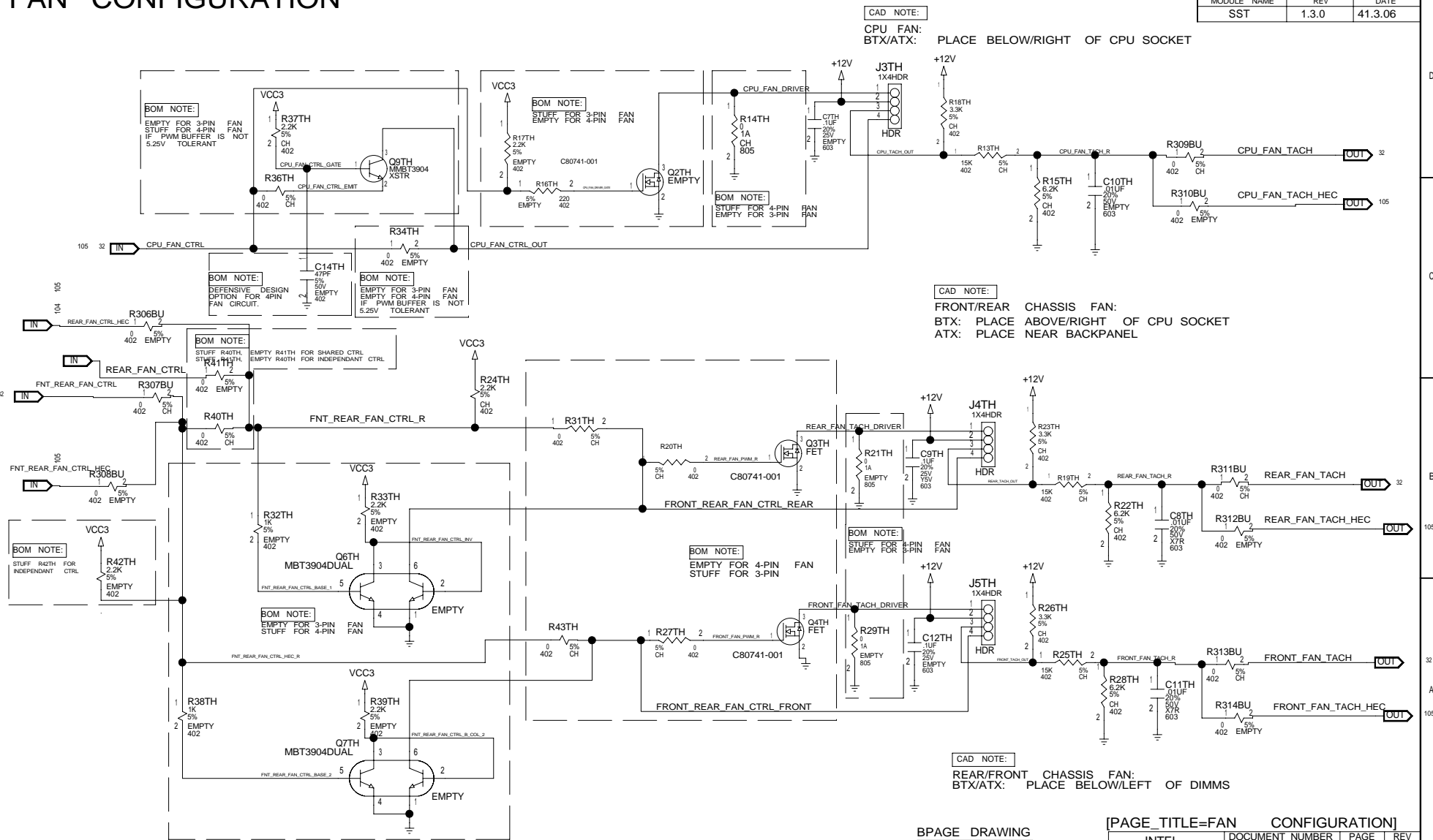
[PAGE_TITLE=SST SENSOR]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxx	PAGE 76	REV 3.01
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CUSTOM TEXT 2 BPAGE

FAN CONFIGURATION

MODULE REV DETAILS		
MODULE NAME	REV	DATE
SST	1.3.0	41.3.06



BPAGE DRAWING

frostburg_fabc.sch_1.77
Sun Mar 18 18:44:40 2007

[PAGE_TITLE=FAN CONFIGURATION]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxx	PAGE 77	P 3.
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CUSTOM TEXT²BPAGE

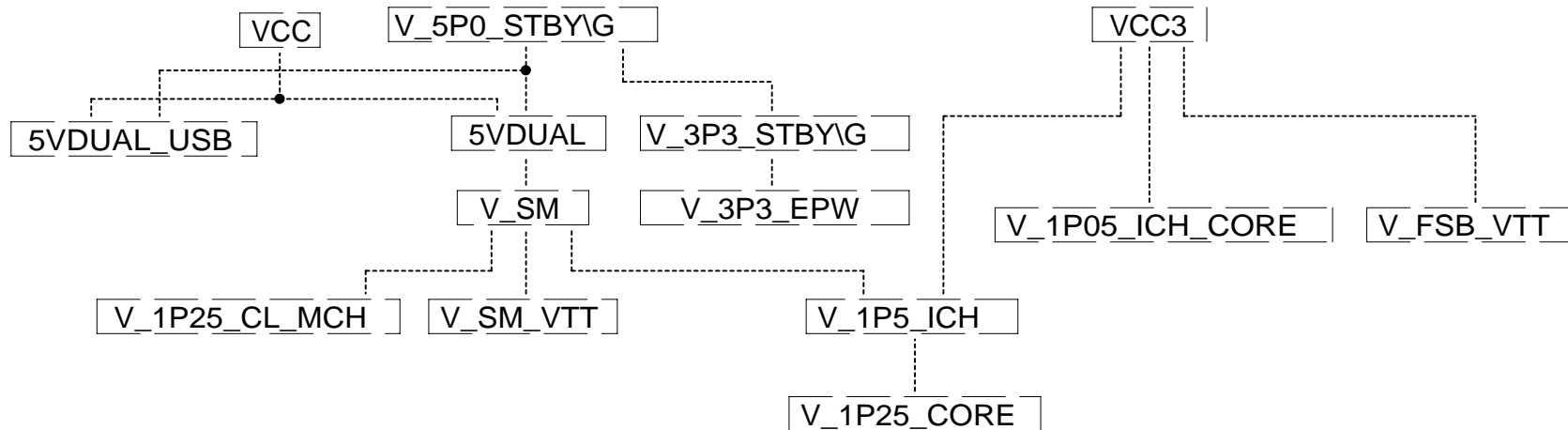
CR-78 :g @FROSTBURG_FABC_LB.FROSTBURG_FABC(SPH_1)-PAGE78		6	5	4	3	2	1								
D	<div>DESIGN NOTE: PB MOUNTING HOLE</div> <div><div>J1PB MTG_HOLE NC9 EMPTY</div><div>J8PB MTG_HOLE NC9 EMPTY</div><div>J9PB MTG_HOLE NC9 EMPTY</div><div>J2PB MTG_HOLE NC9 EMPTY</div><div>J7PB MTG_HOLE NC9 EMPTY</div><div>J10PB MTG_HOLE NC9 EMPTY</div><div>J4PB MTG_HOLE NC9 EMPTY</div><div>J6PB MTG_HOLE NC9 EMPTY</div><div>J11PB MTG_HOLE NC9 EMPTY</div><div>J3PB MTG_HOLE NC9 EMPTY</div><div>J5PB MTG_HOLE NC9 EMPTY</div></div>						<div>MODULE REV DETAILS</div> <table><thead><tr><th>MODULE NAME</th><th>REV</th><th>DATE</th></tr></thead><tbody><tr><td></td><td></td><td></td></tr></tbody></table>		MODULE NAME	REV	DATE				
	MODULE NAME	REV	DATE												
	C														
B	<div>DESIGN NOTE: LABELS</div>														
	<div><div>1500X150_TARGET LB6PB LABEL A30094-001</div><div>DESIGN NOTE: 200956-001 (NO CONCEPT MODEL): CE MARK SHOULD BE COVERED WITH BLANK WHITE LABEL UNTIL CERTIFIED (MAY NOT BE ON RVP DESIGNS) 628492-001: FCC MARK SHOULD BE COVERED WITH BLANK WHITE LABEL UNTIL CERTIFIED (MAY NOT BE ON RVP DESIGNS) 622954-001: C-TICK MARK SHOULD BE COVERED WITH BLANK WHITE LABEL UNTIL CERTIFIED (MAY NOT BE ON RVP DESIGNS) KOREAN CERT (NO IPN, NO CONCEPT MODEL) SHOULD BE COVERED WITH BLANK WHITE LABEL UNTIL CERTIFIED (NOT ON RVP DESIGNS)</div><div>CAD NOTE: LB6PB: PLACE KOZ TARGET NEAR CPU AND DIMMS FOR BUILD/WOC NOTES</div></div>														
A	<div><div>1375X250_TARGET LB5PB LABEL A19177-001</div><div>DESIGN NOTE: LB5PB: ISN BLANK LABEL AND KOZ</div></div> <div><div>EMPTY LB20PB LABEL 1000X187</div><div>DESIGN NOTE: SILK TARGET FOR PRODUCT CODE LABEL</div></div>														
						<div>CHINA_ROHS LB25PB LABEL EMPTY</div> <div>VCCI_SILK LB17PB LABEL EMPTY</div> <div>E210882_LB LB16PB LABEL EMPTY</div> <div>UL LABEL LB15PB LABEL EMPTY</div> <div>MIC_CPU LB13PB LABEL EMPTY</div> <div>FCCSILK LB12PB LABEL EMPTY</div> <div>CE LABEL LB11PB LABEL EMPTY</div> <div>EMPTY LB7PB LABEL INTEL_LOGO</div>	<div>B2_SILK LB19PB LABEL EMPTY</div> <div>SILK LB9PB C-TICK EMPTY</div> <div>BSMI_SILK LB10PB LABEL EMPTY</div> <div>E2_SILK LB18PB LABEL EMPTY</div> <div>E1_SILK LB2PB LABEL EMPTY</div> <div>PB_FREE_2LI LB3PB LABEL EMPTY</div> <div>CANADA LB21PB LABEL EMPTY</div>								
<div>[PAGE_TITLE=MTG HOLES/LABELS]</div> <div><div>BPAGE DRAWING frostburg_fabc.sch_1.78 Sun Mar 18 18:44:42 2007</div><table><thead><tr><th>INTEL CONFIDENTIAL</th><th>DOCUMENT_NUMBER xxxxxxx</th><th>PAGE 78</th><th>REV 3.01</th></tr></thead><tbody><tr><td colspan="2">CUSTOM TEXT² BPAGE</td><td colspan="2">1</td></tr></tbody></table></div>							INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 78	REV 3.01	CUSTOM TEXT ² BPAGE		1		
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 78	REV 3.01												
CUSTOM TEXT ² BPAGE		1													
8		7		6		5		4		3		2		1	

CR-79 : 8 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(SPH_1):PAGE79

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_B_ATX	06.12.2	2/8/07

CORE VR MODULE

V_SM POWERED BY 5VDUAL
 V_SM_VTT POWERED BY V_SM
 V_1P5_ICH POWERED BY V_SM OR VCC3
 V_1P25_CORE POWERED BY V_1P5_ICH
 V_1P05_ICH_CORE POWERED BY VCC3
 V_FSB_VTT POWERED BY VCC3
 V_1P25_CL_MCH POWERED BY V_SM
 5VDUAL_USB POWERED BY V_5P0_STBY\G AND VCC
 5VDUAL POWERED BY V_5P0_STBY\G AND VCC
 V_3P3_STBY\G POWERED BY V_5P0_STBY\G
 V_3P3_EPW POWERED BY V_3P3_STBY\G

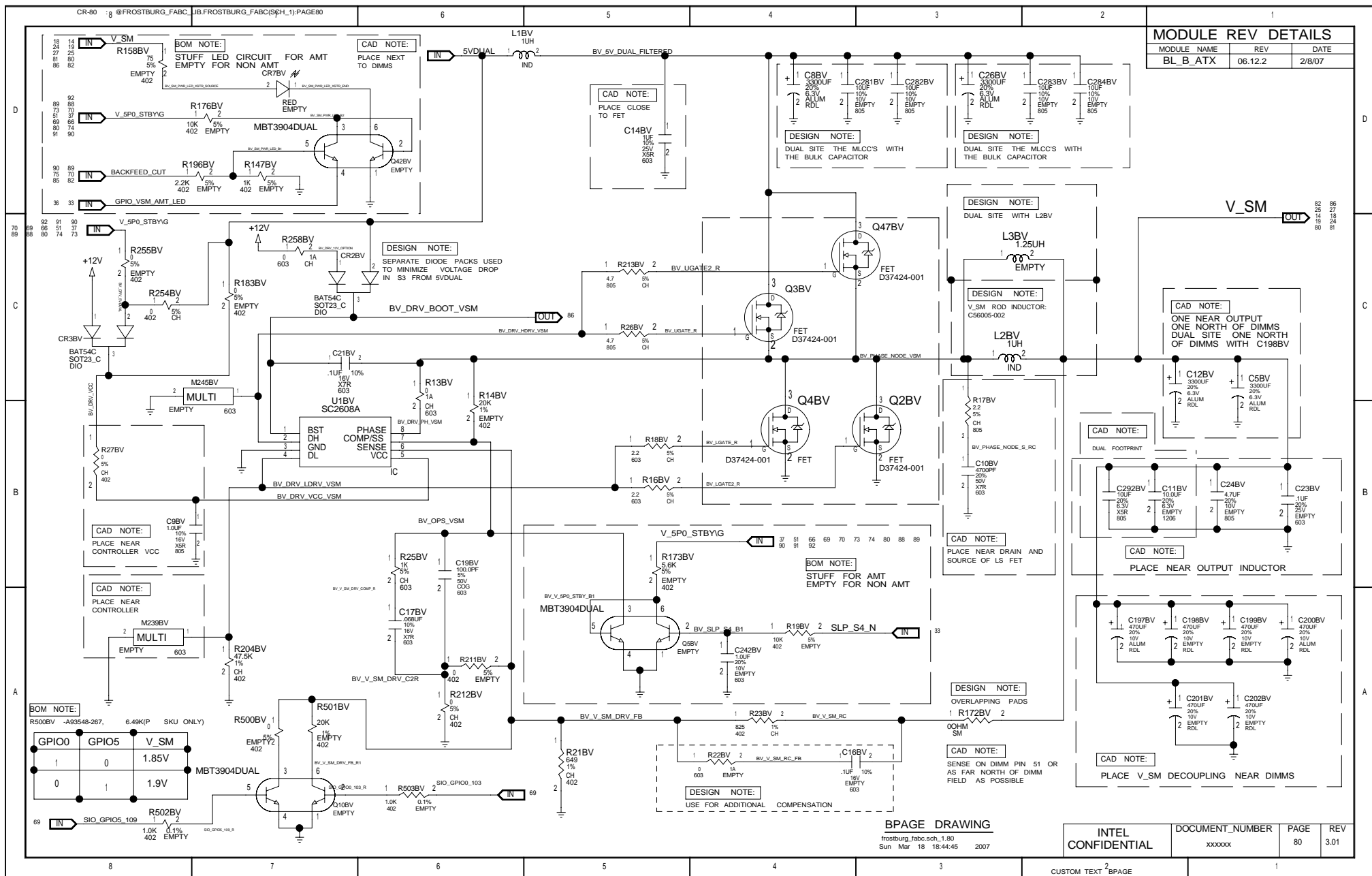


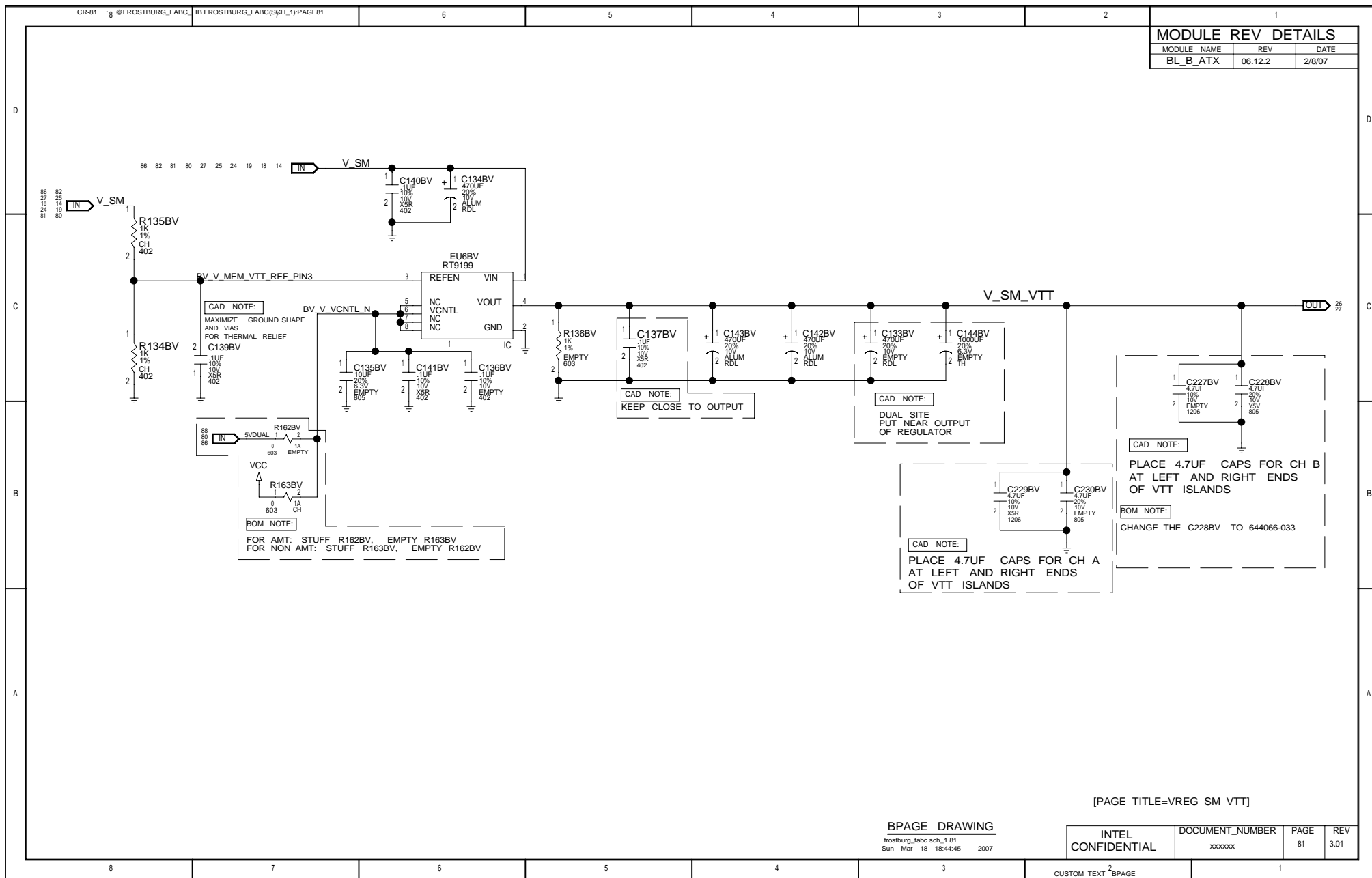
BPAGE DRAWING

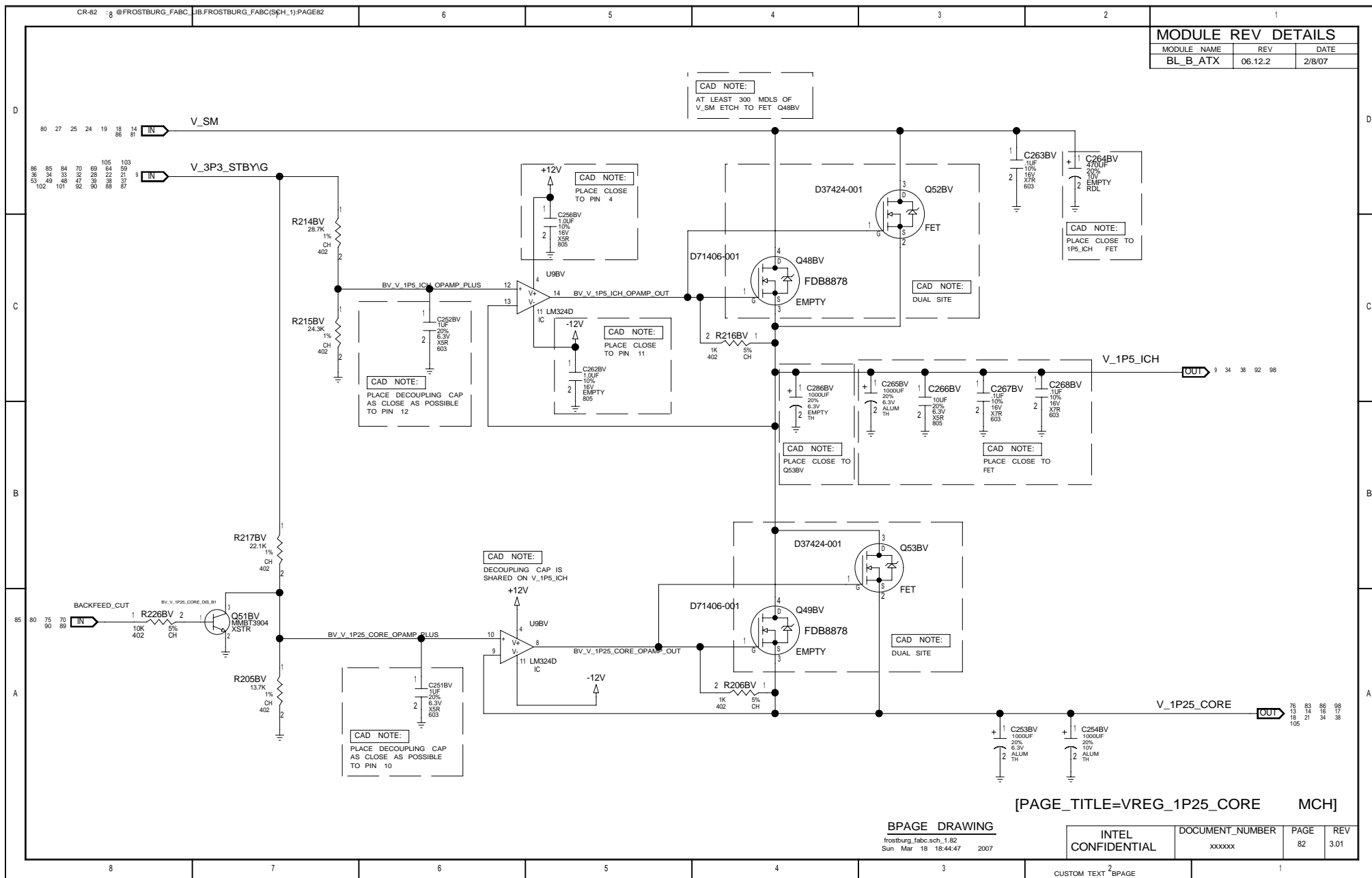
frostburg_fabc.sch, 1.79
Sun Mar 18 18:44:43 2007

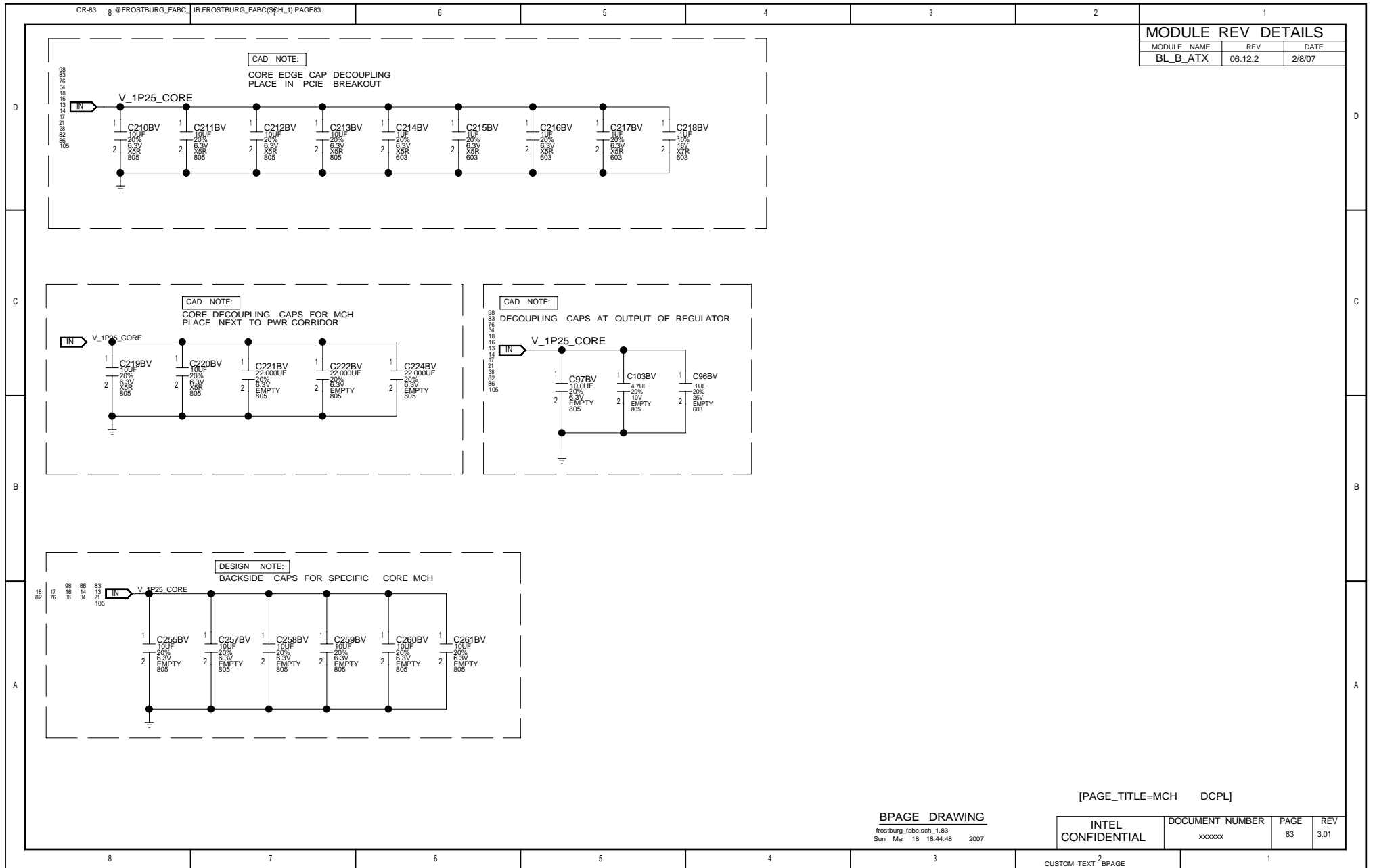
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 79	REV 3.01
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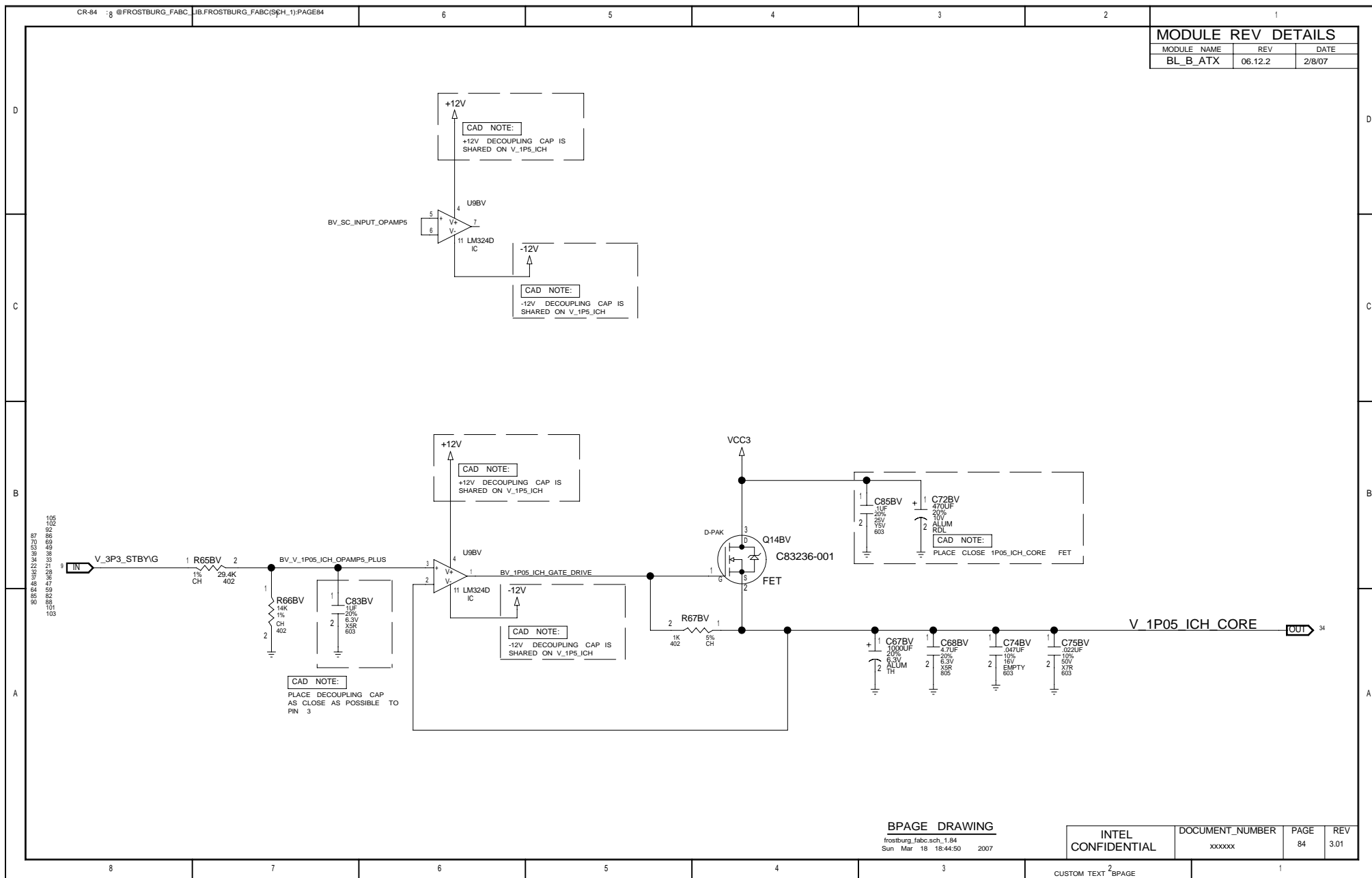
CUSTOM TEXT² BPAGE

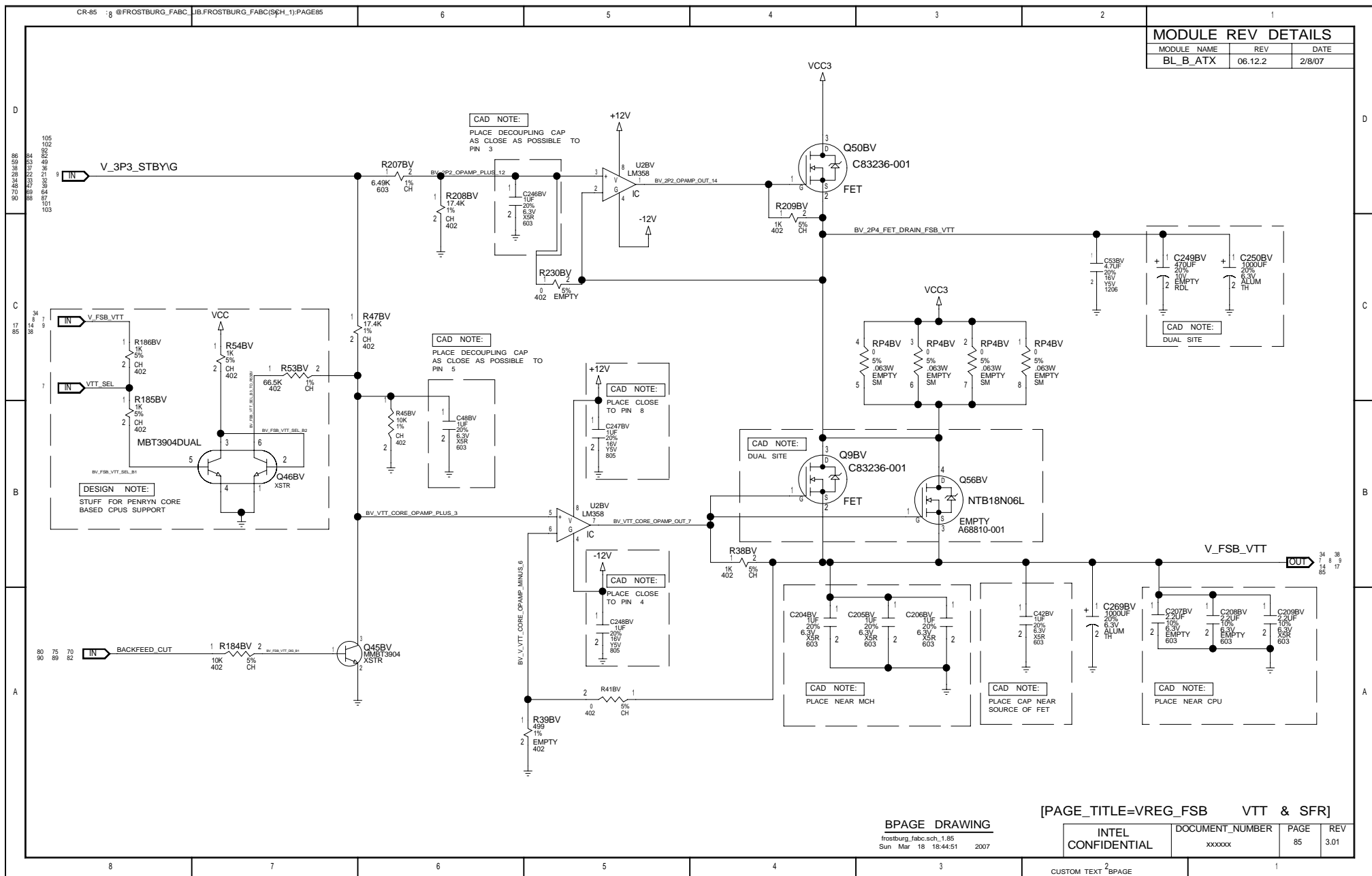


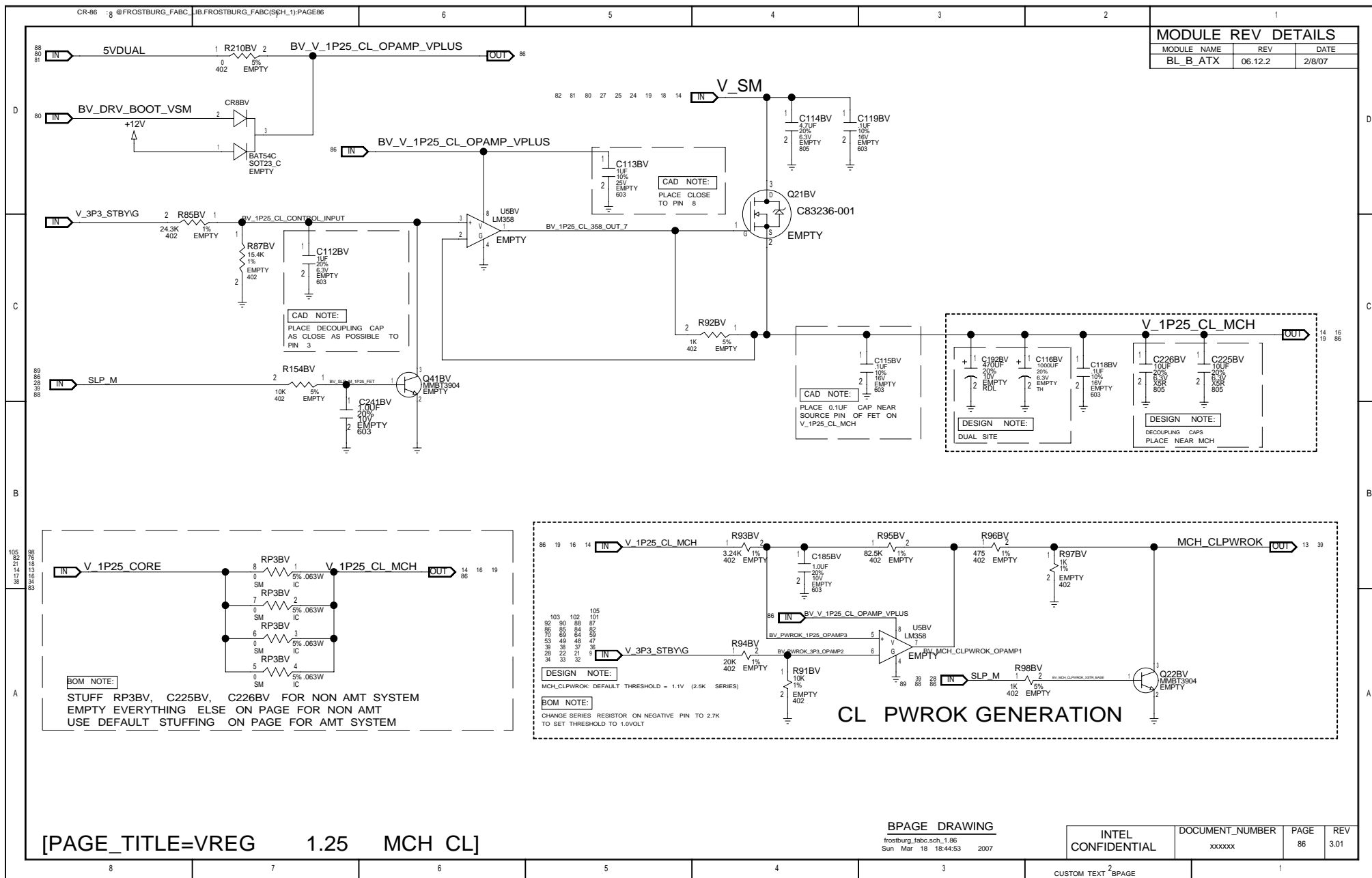


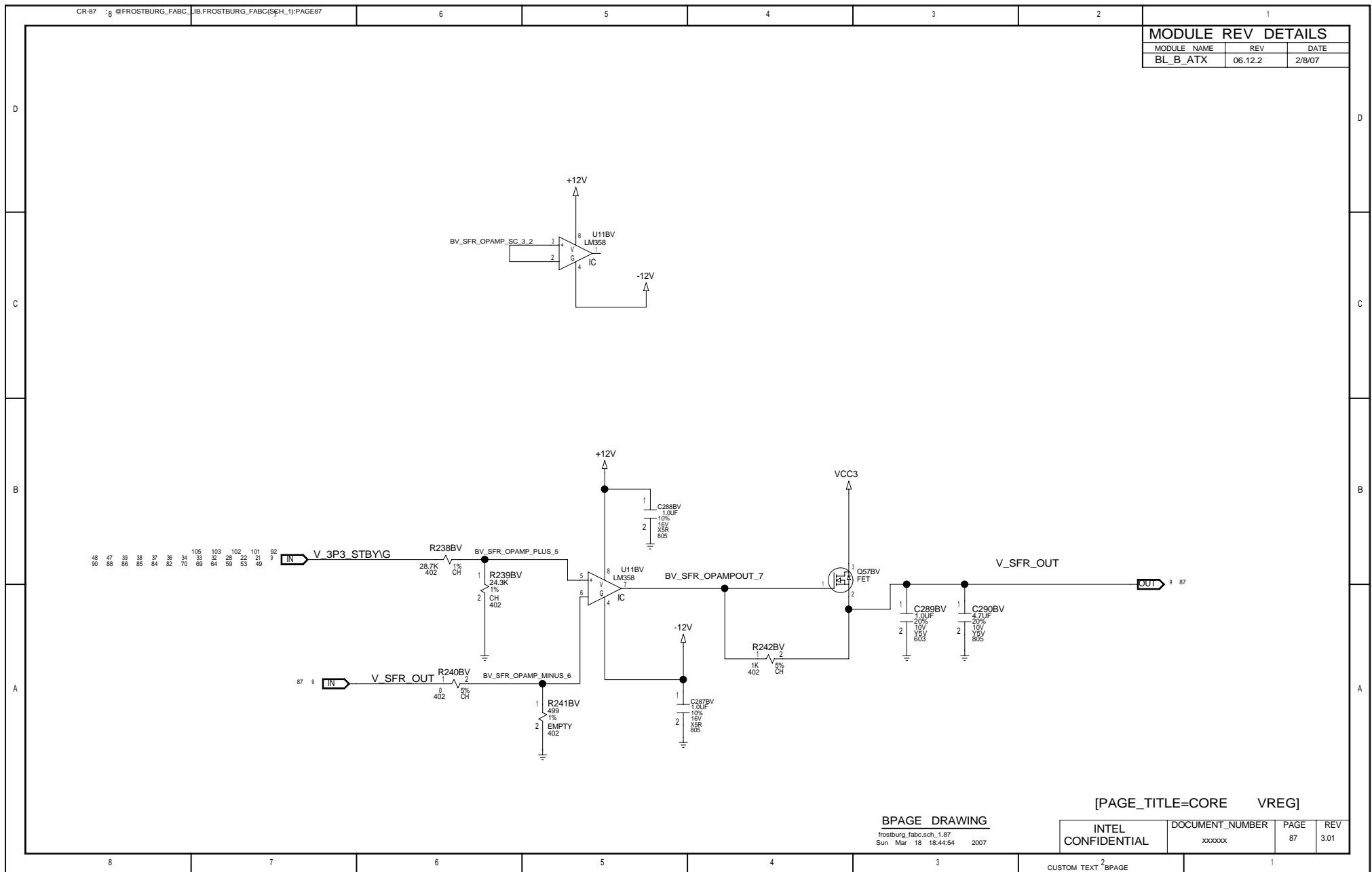


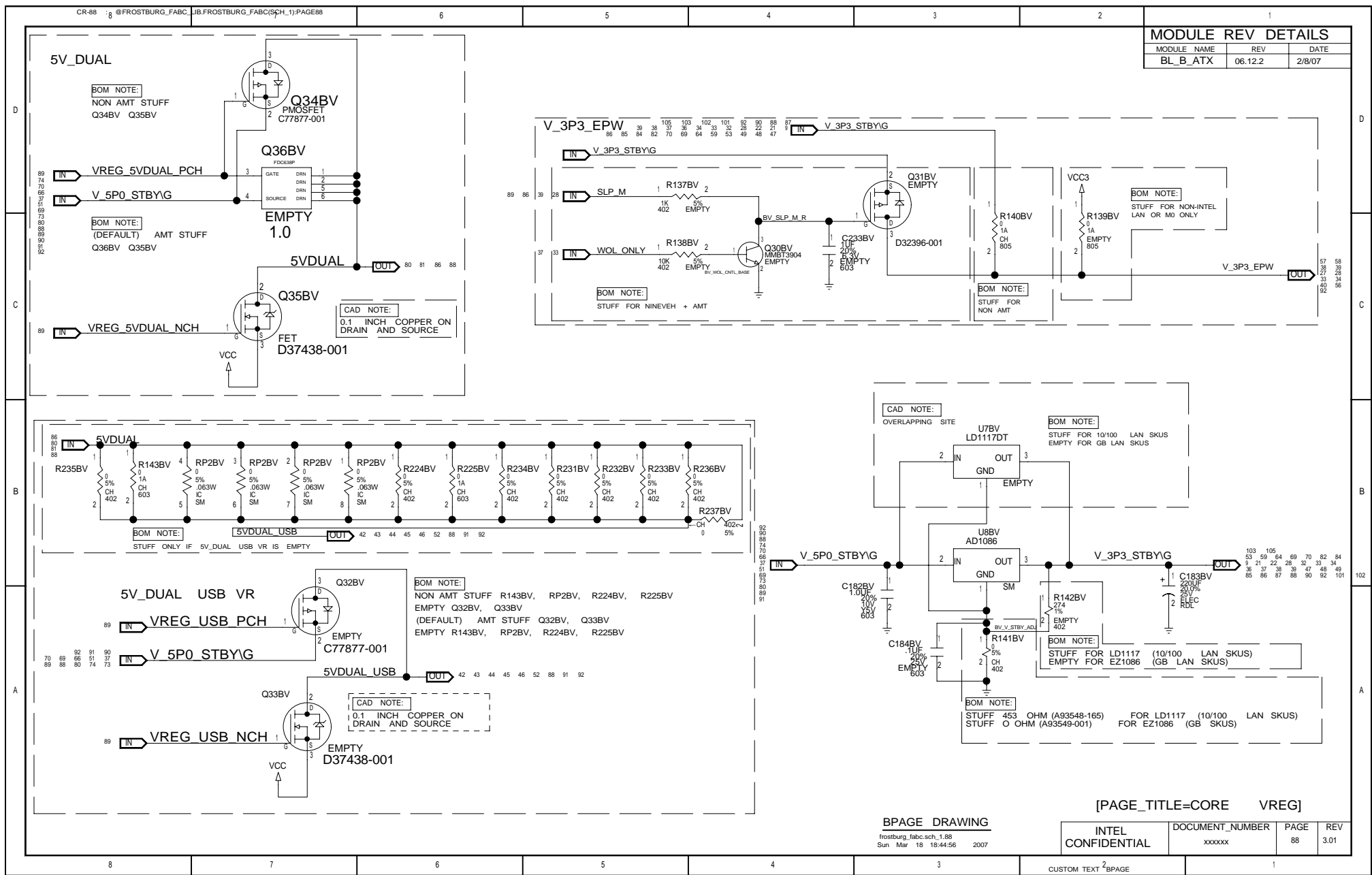


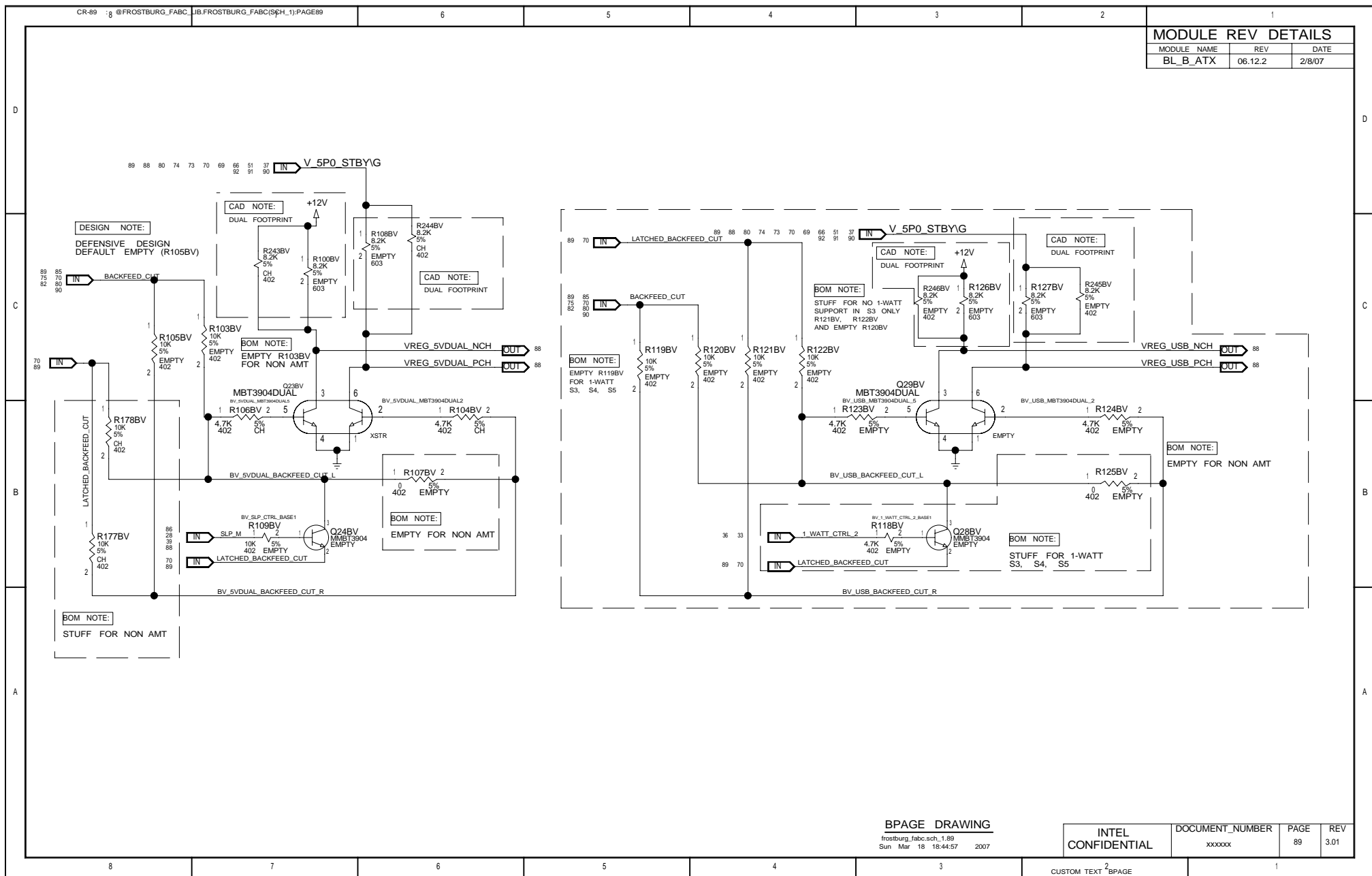


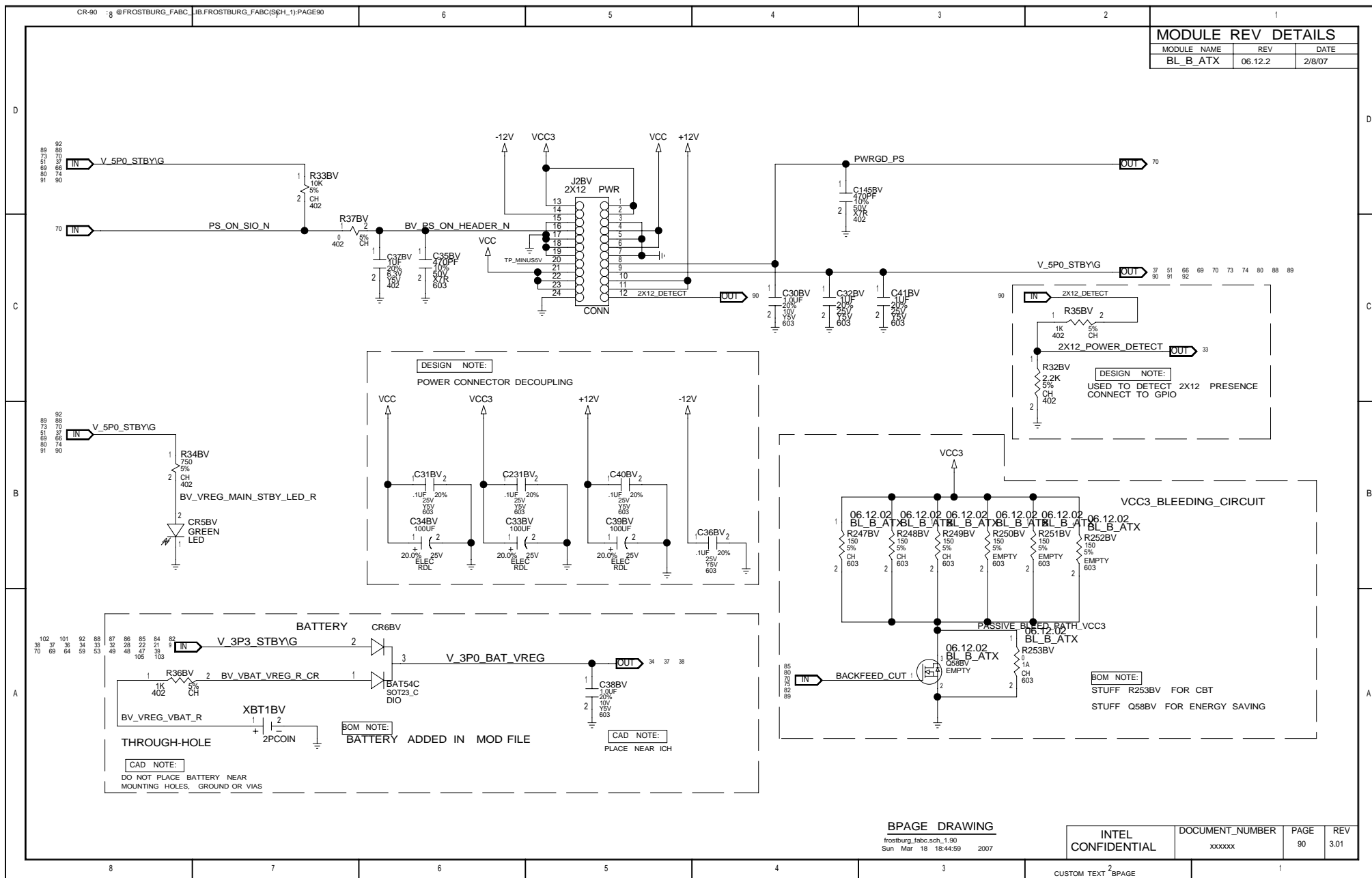


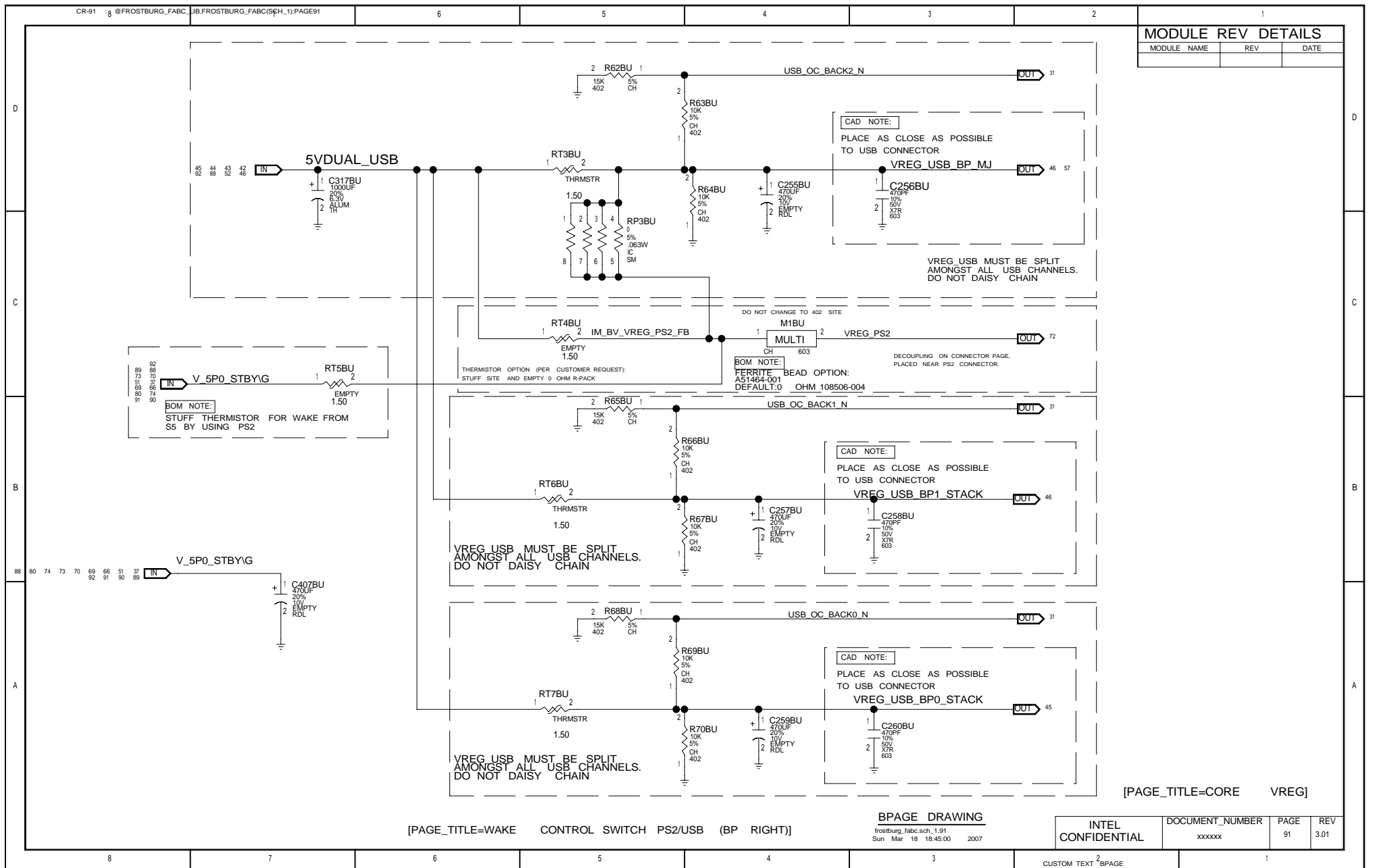


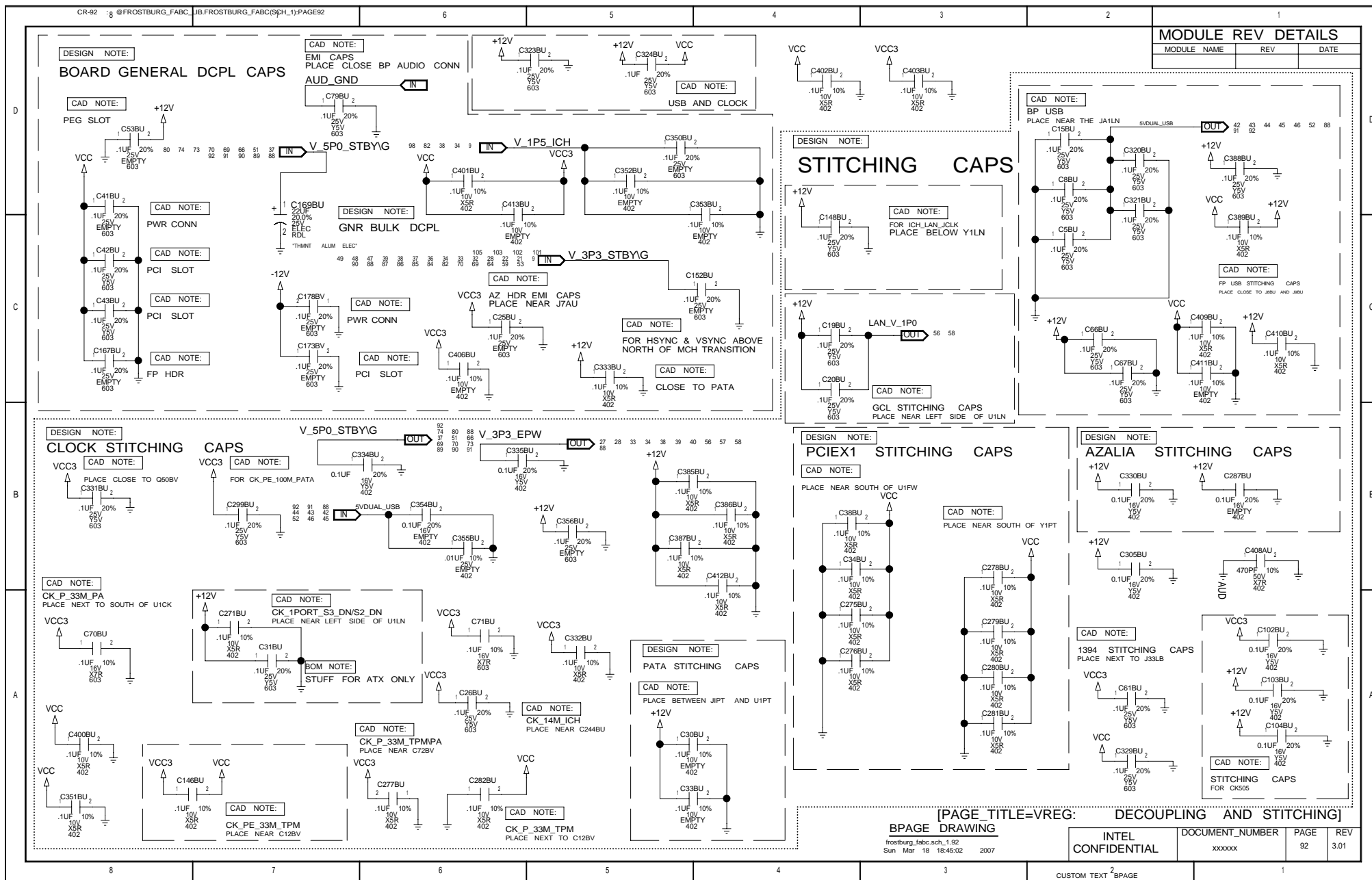


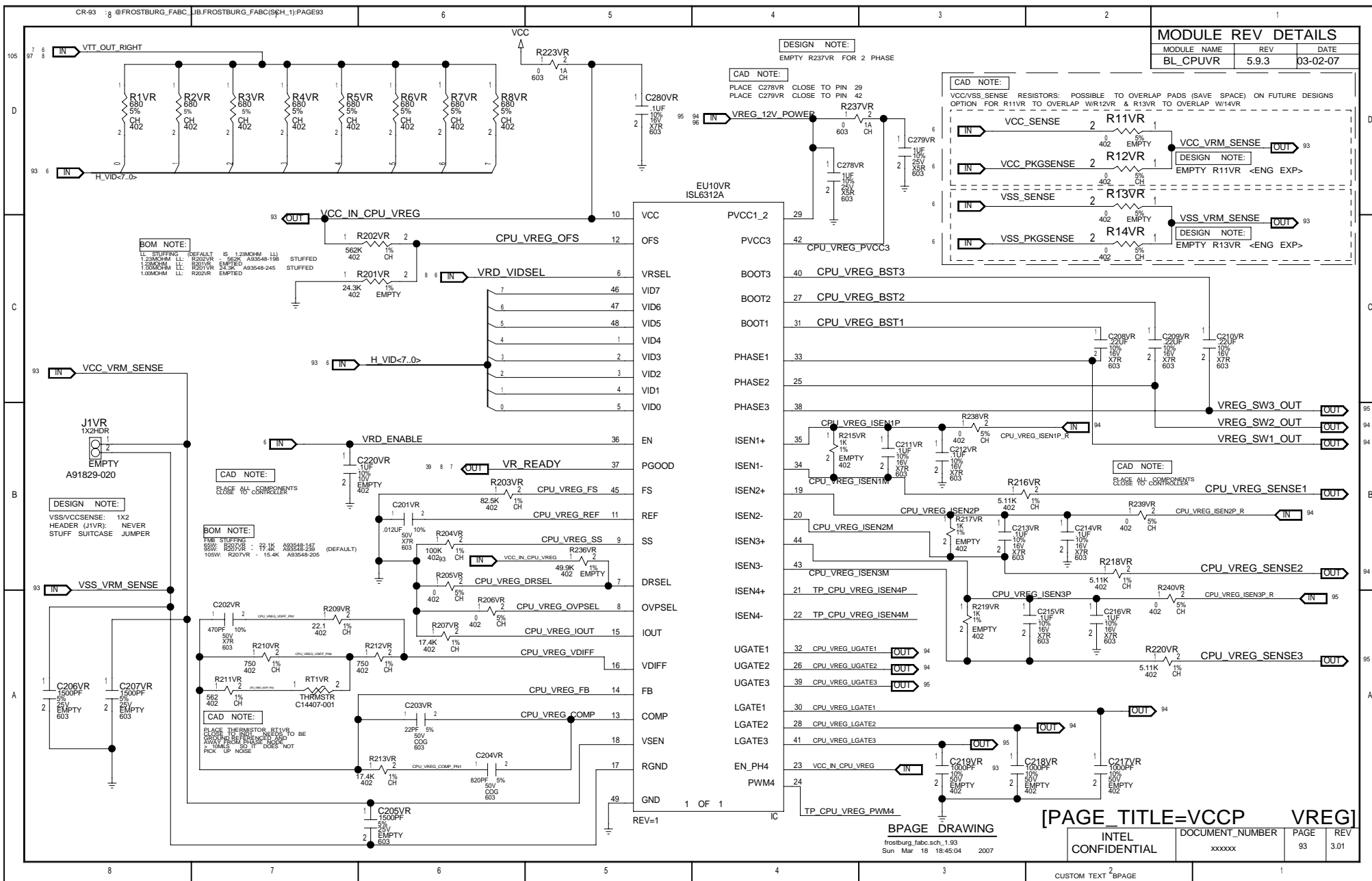


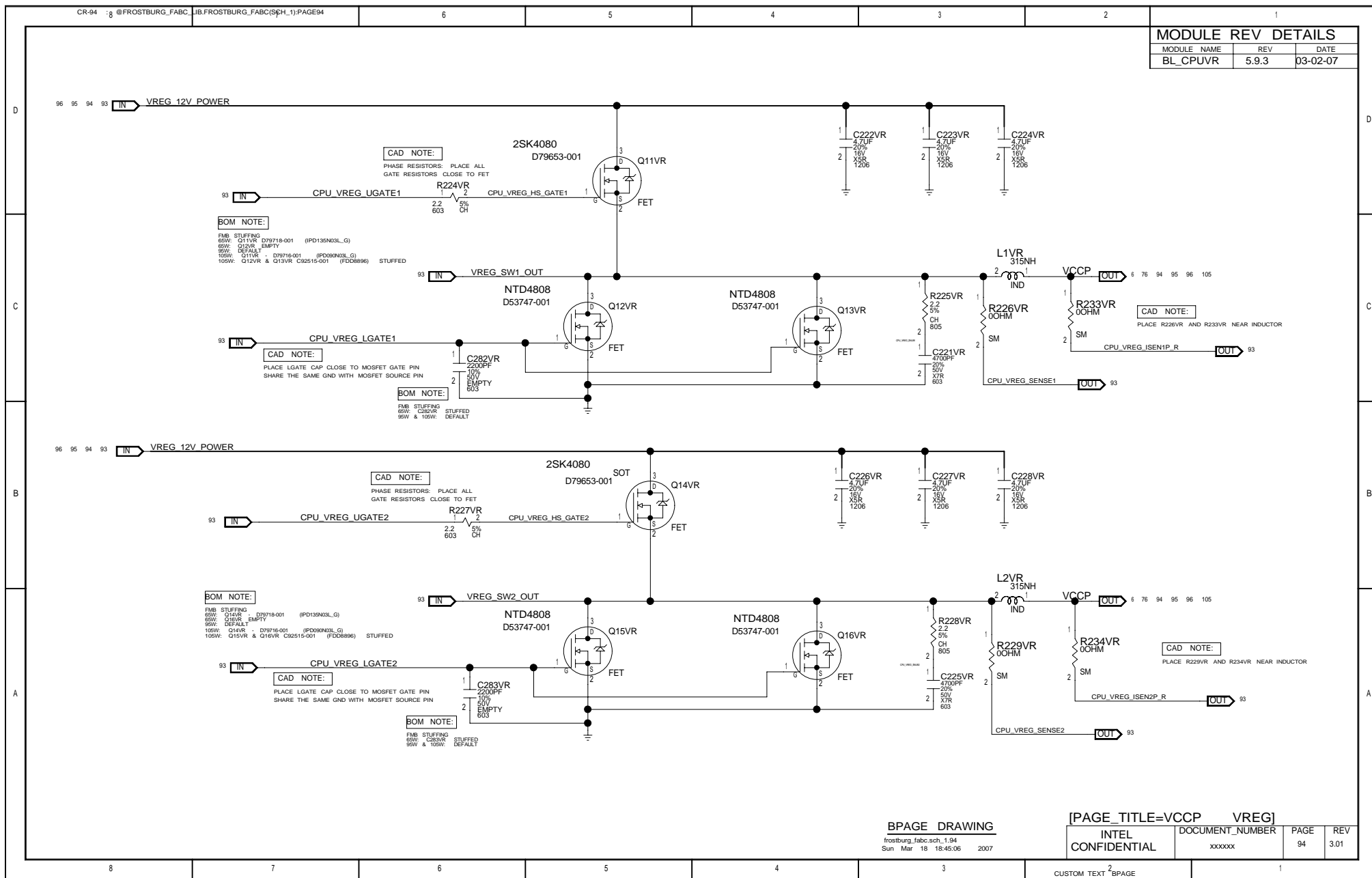


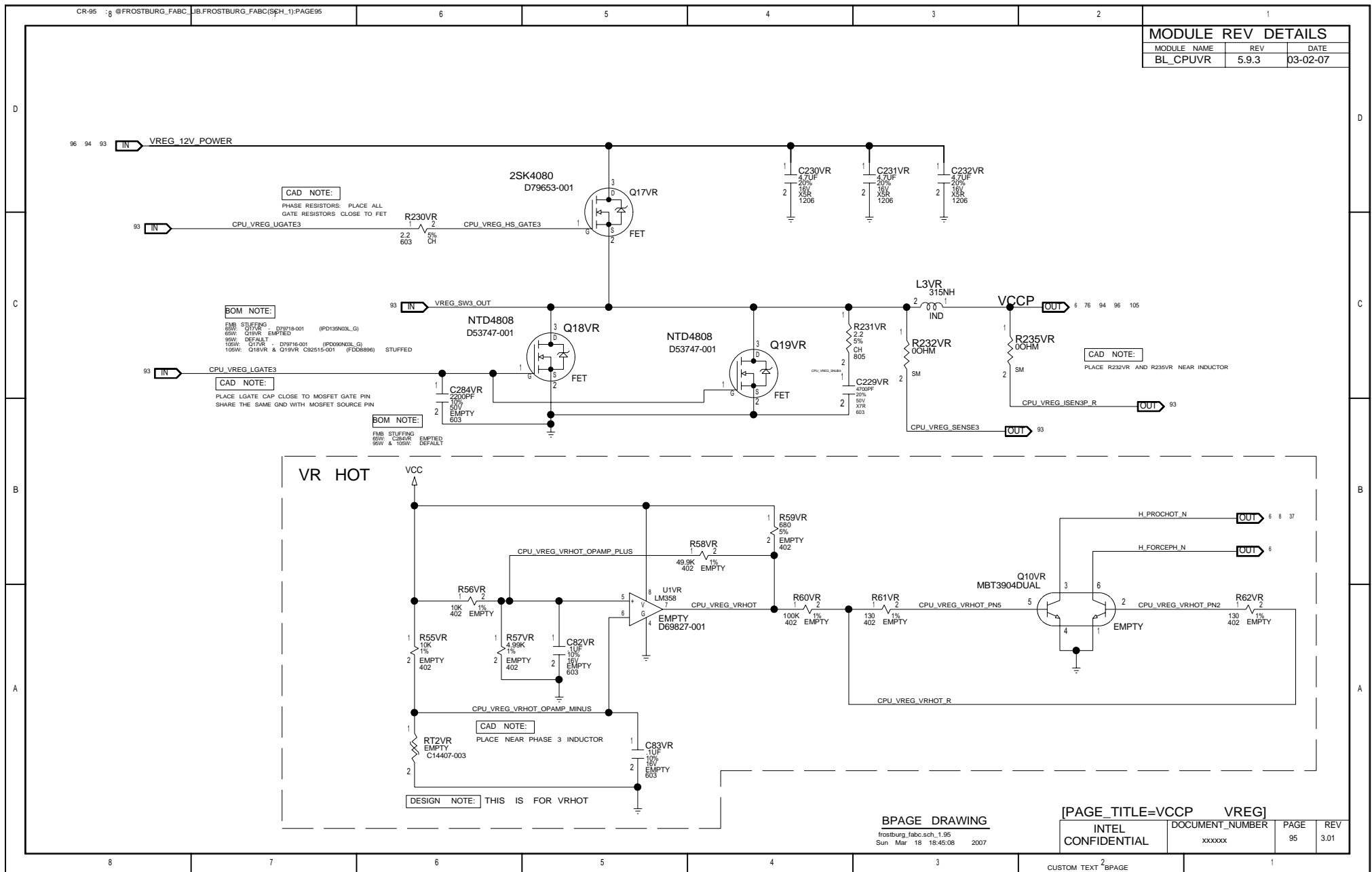


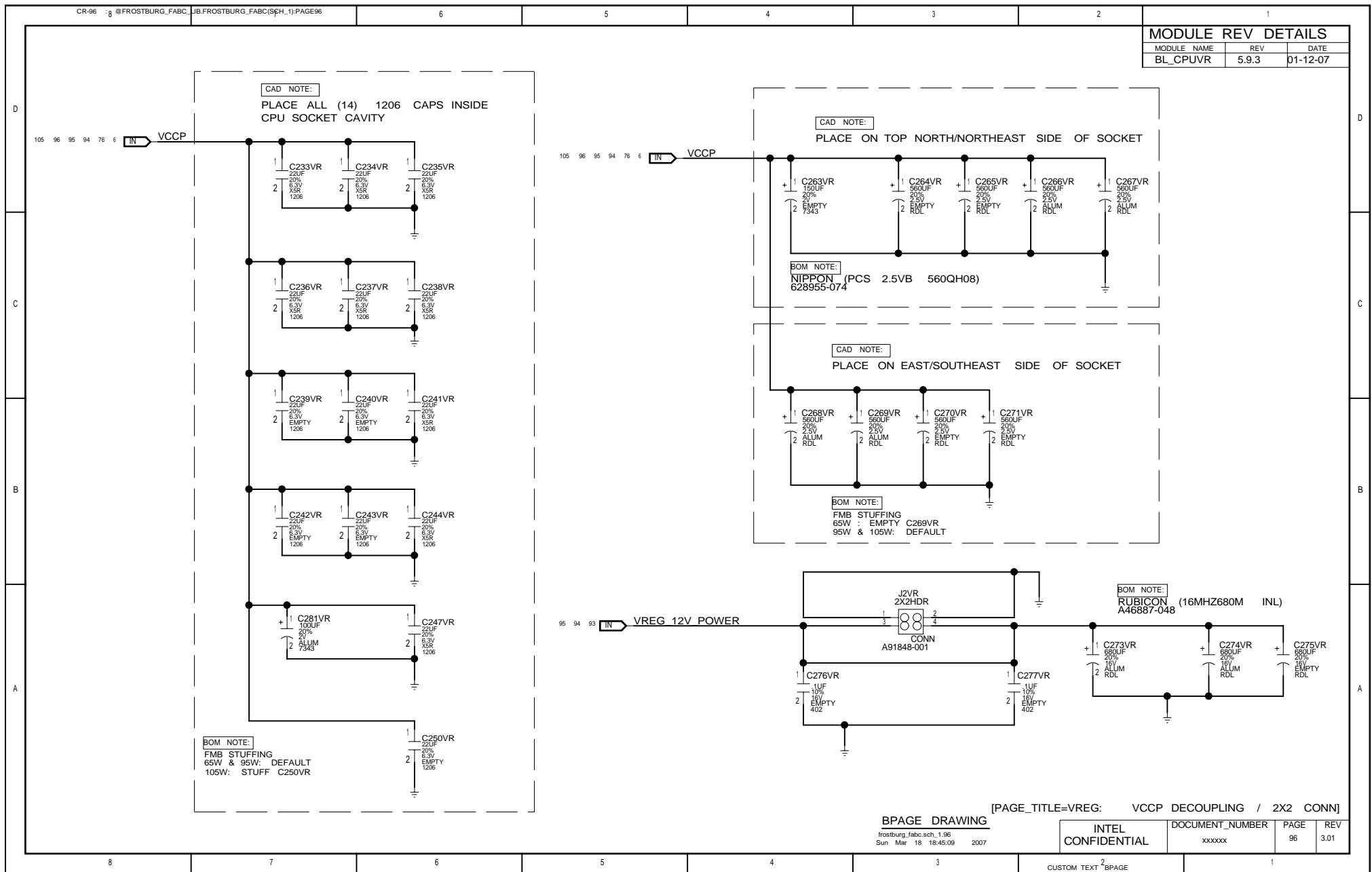










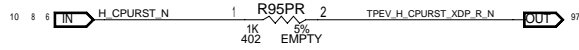


BW_ATX_CORE

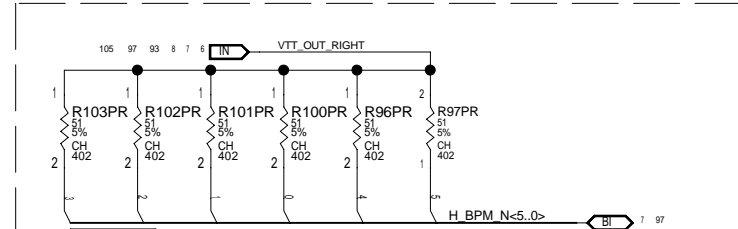
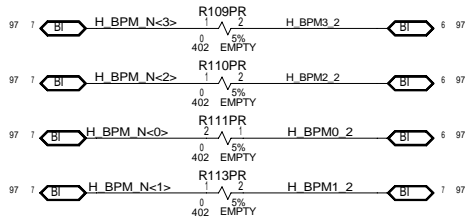
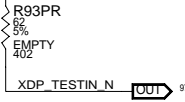
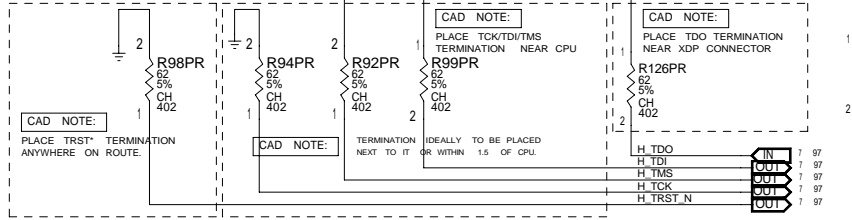
CR-97 - 8 @FROSTBURG_FABC JB.FROSTBURG_FABC(Sch_1)-PAGE97

MODULE REV DETAILS

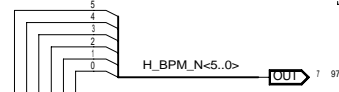
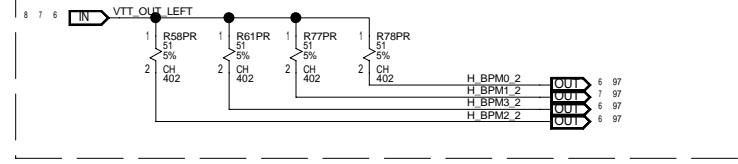
MODULE NAME	REV	DATE
BW_ATX_CORE	1.06.00	5-5-06



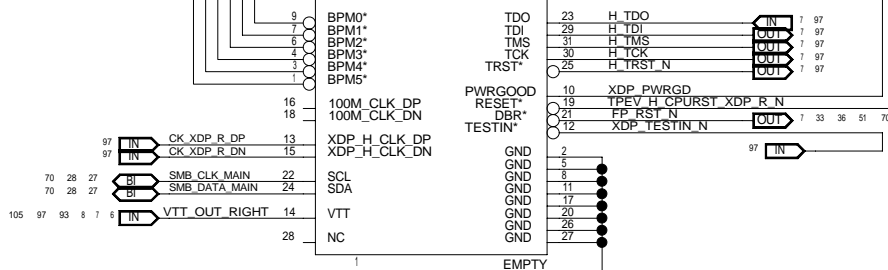
105 97 93 8 7 6 IN VTT_OUT_RIGHT



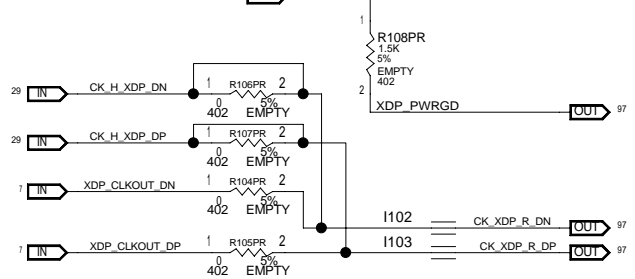
CAD NOTE: PLACE BPM TERMINATION NEAR CPU



J2BC XDP_SSA BOM NOTE: STUFF FOR CRB BOARD



105 97 93 8 7 6 IN VTT_OUT_RIGHT



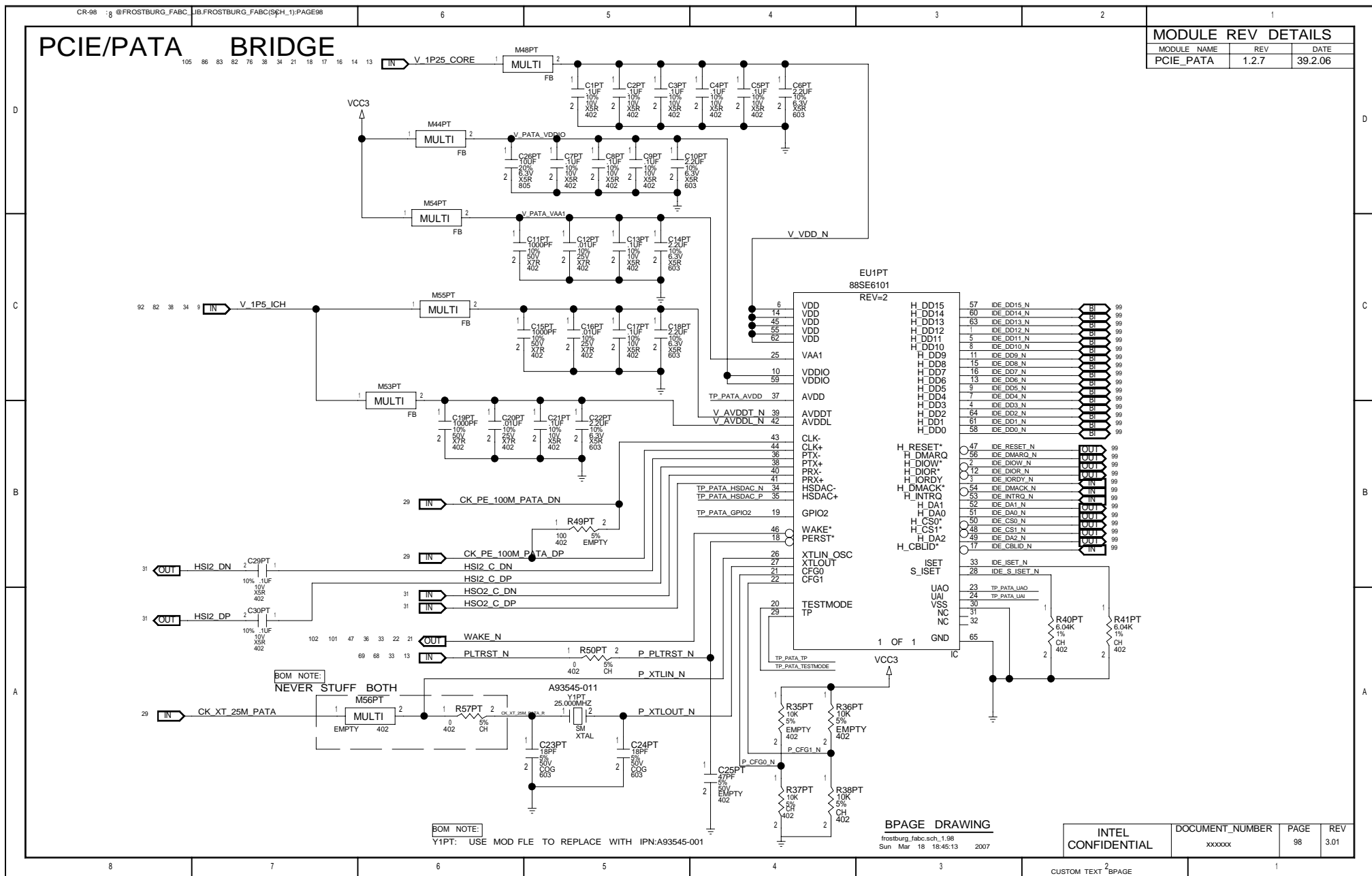
BPAGE DRAWING

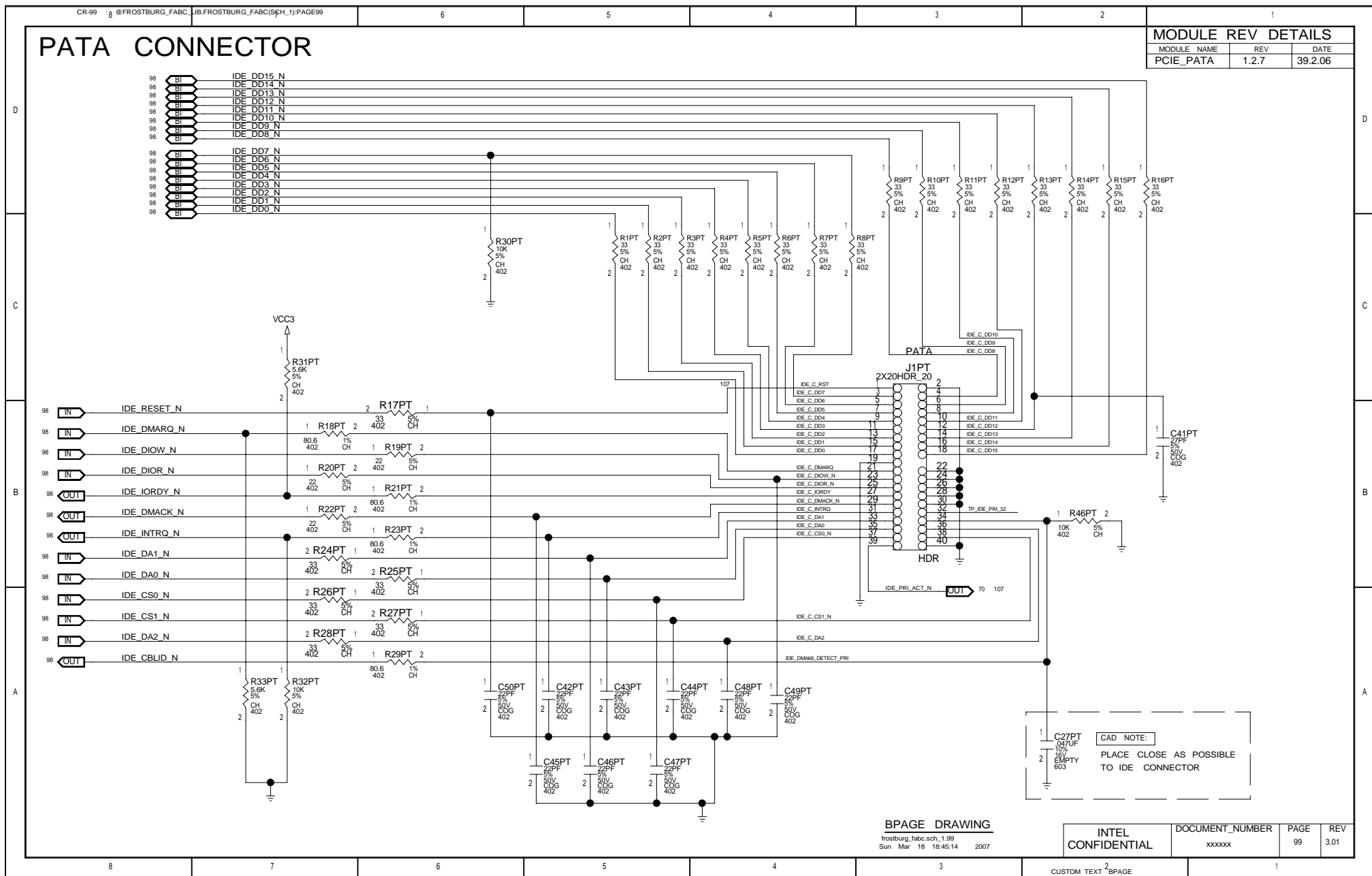
frostburg_fabc.sch_1.97
Sun Mar 18 18:45:11 2007

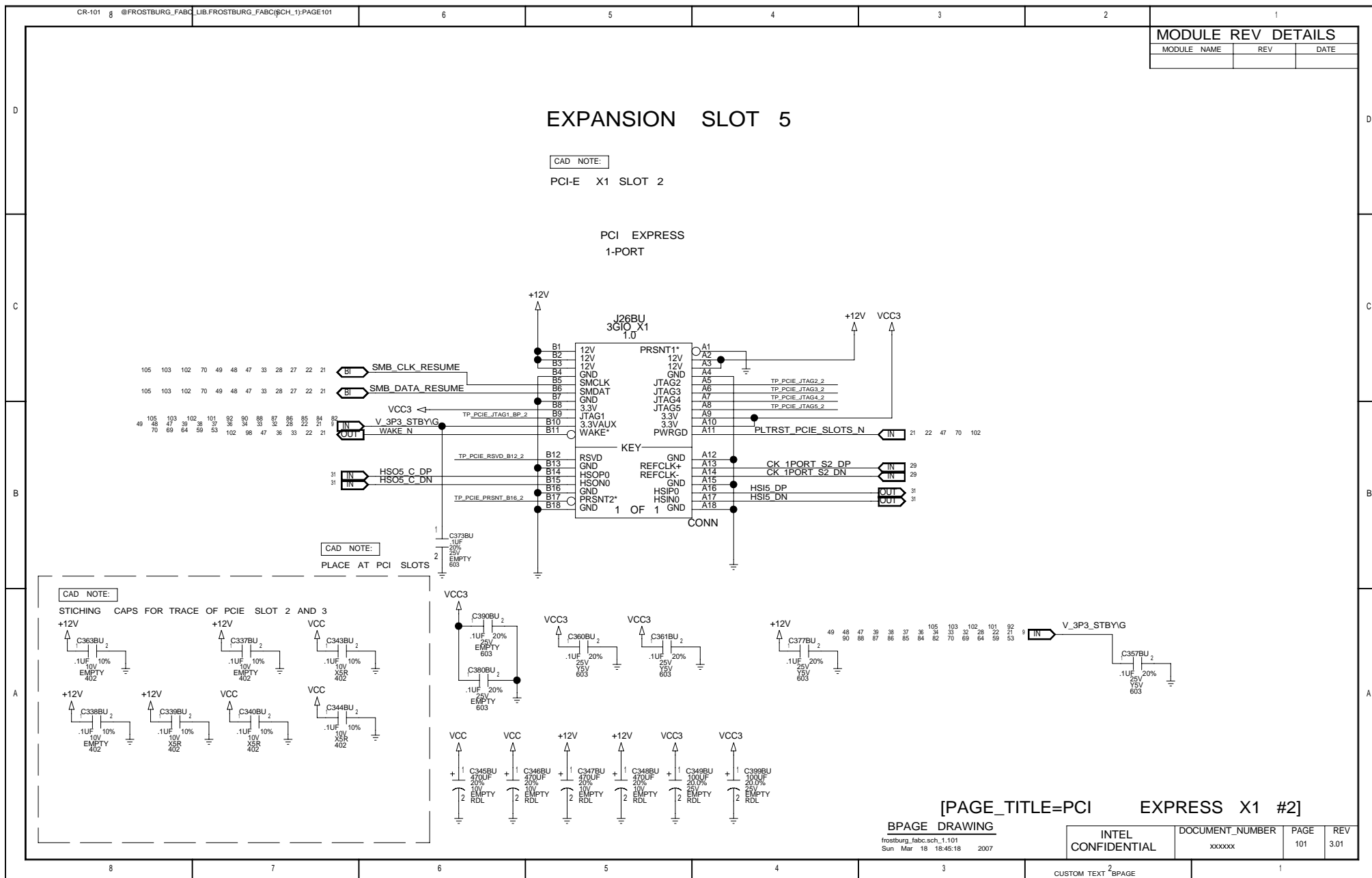
[PAGE_TITLE=PRIMARY XDP-LITE]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	xxxxxxx	97	3.01

CUSTOM TEXT BPAGE







CR-102 g @FROSTBURG_FABCD LIB:FROSTBURG_FABCI(SCH_1):PAGE102

MODULE REV DETAILS

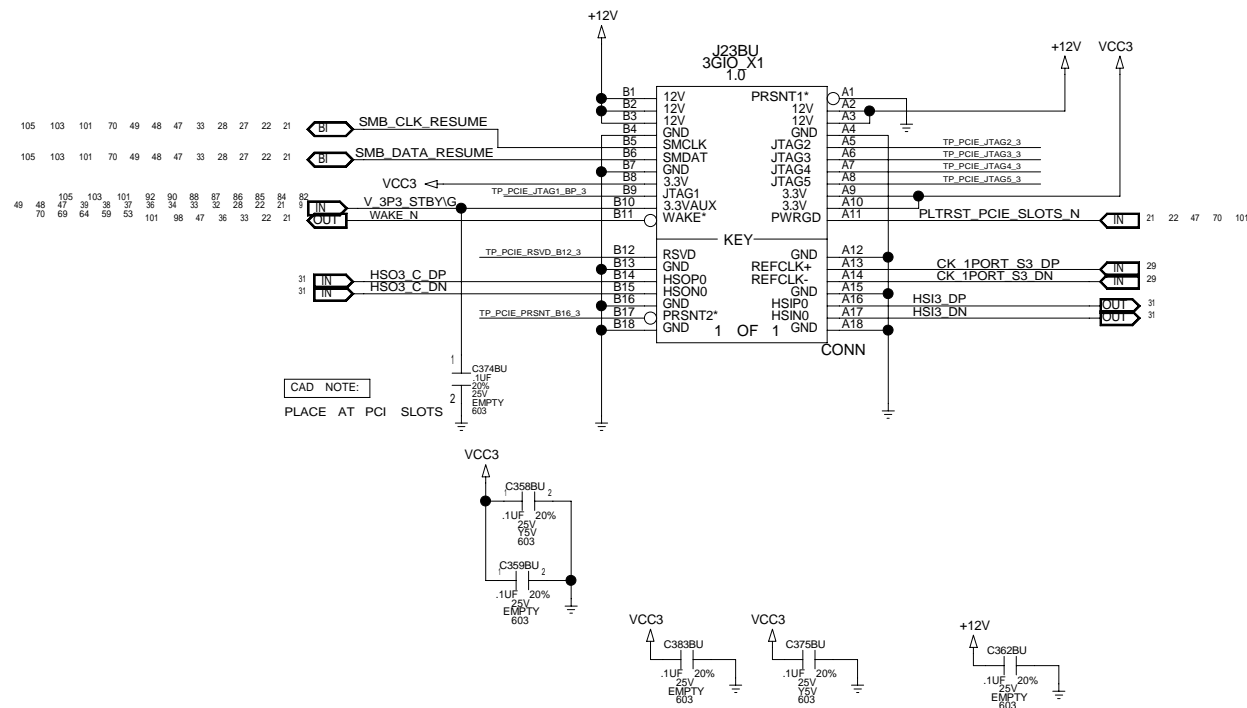
MODULE NAME	REV	DATE

EXPANSION SLOT 6

CAD NOTE:

PCI-E X1 SLOT 3

PCI EXPRESS
1-PORT



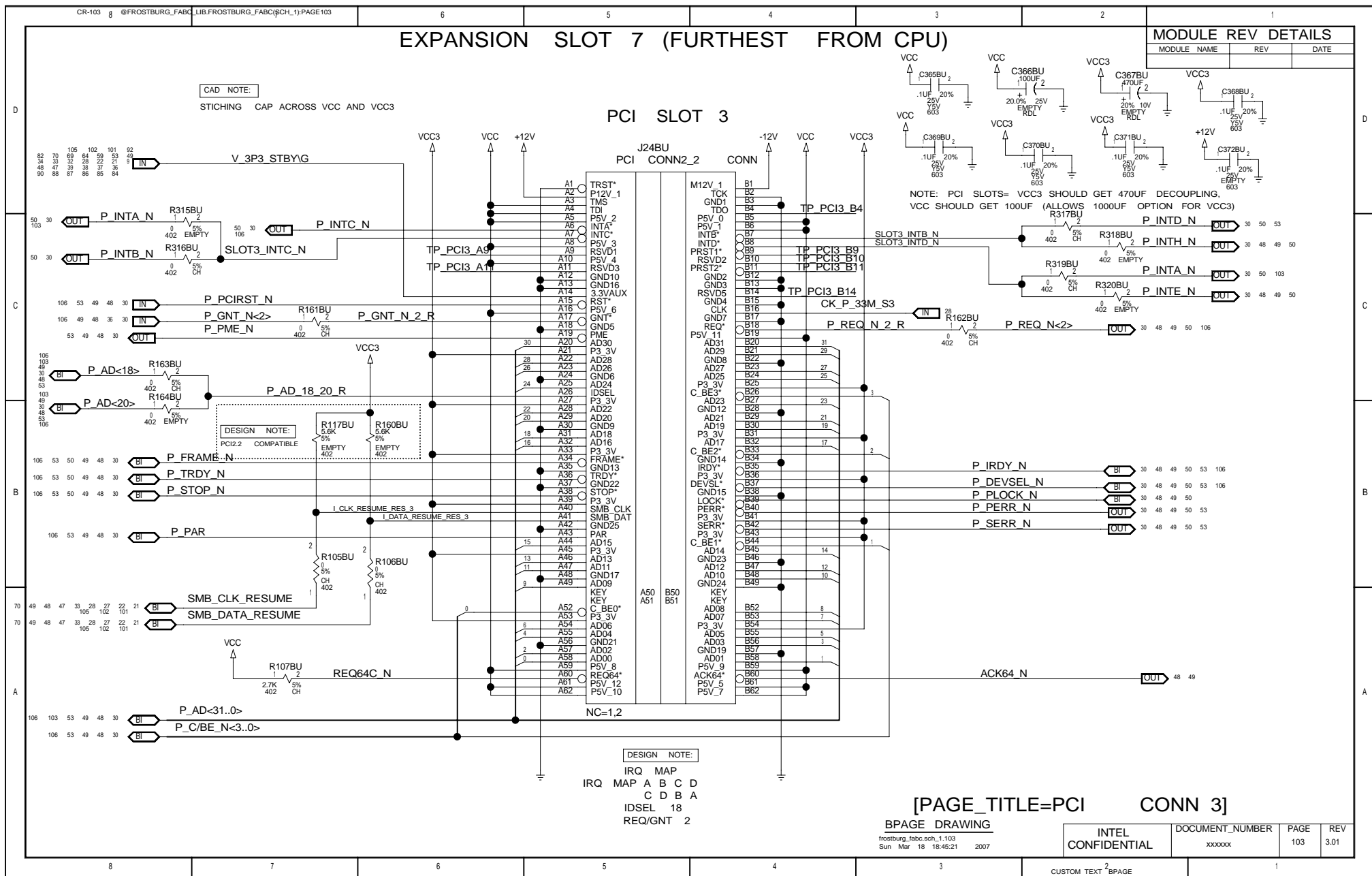
[PAGE_TITLE=PCI EXPRESS X1 #3]

BPAGE DRAWING

frostburg_fabci.sch, 1.102
Sun Mar 18 18:45:19 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 102	REV 3.01
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CUSTOM TEXT 2 BPAGE

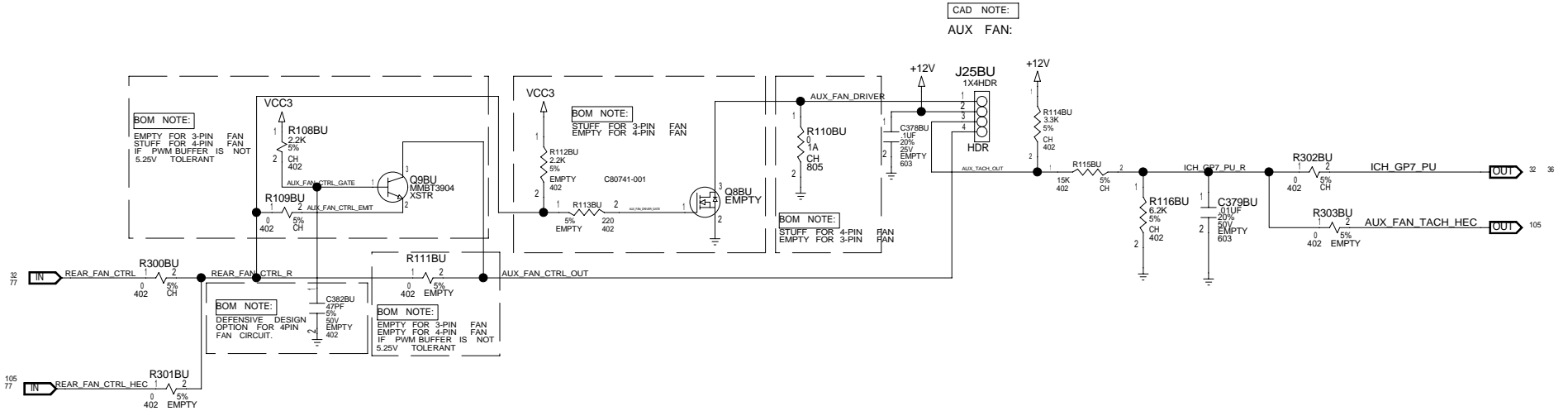


CR-104 g @FROSTBURG_FAB0 LIB:FROSTBURG_FABC(SCH_1):PAGE104

AUX FAN CONFIGURATION

MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=AUX FAN CONFIGURATION]

BPAGE DRAWING

frostburg_fabc.sch, 1.104
Sun Mar 18 18:45:24 2007

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CUSTOM TEXT 2 BPAGE

